HIGH-EFFICIENCY 2-STAGE MULTIPHASE SWITCHED-CAPACITOR CONVERTER VIA VARIABLE-PHASE AND PWM CONTROL

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Abstract: A closed-loop switched-capacitor (SC) converter based on voltage-mode two-stage multiphase voltage doubler (MPVD) is proposed by combining four-level pulse-width-modulation (PWM) control for high-efficiency low-power DC-DC step-up/down conversion. Basically, SC converter needs no magnetic element, so VLSI fabrication is promising future. In addition, because MPVD scheme can obtain the high voltage gain just by the least number of pumping capacitors, the fabrication area is saved more. Here, for the better conversion efficiency, the four-level control is suggested and added into the multiphase operation to change the voltage gain automatically (4x/3x/2x/1x) according to the desired output range. For the better output regulation, the PWM technique is adopted not only to compensate the dynamic error between the practical and desired outputs, but also to reinforce the output robustness against loading variations or source disturbances. In this paper, the relative theoretical analysis and control design are discussed, including four-level MPVD averaging model, steady-state/transient analysis, power conversion efficiency, voltage conversion ratio, ripple percentage, capacitance selection, closed-loop control and stability. Finally, the closed-loop four-level PWM-based MPVD is designed by OrCAD, and then the hardware implementation of MPVD is realized and tested. All the results are illustrated to show the efficacy of the proposed converter.

Keywords: switched-capacitor, multiphase voltage doubler, step-up/down converter, pulse-width-modulation.

1. Introduction

With the coming of portable electronic equipments being popular, some features of power modules are emphasized and asked, such as small volume, light weight, high power density, better power efficiency, and good regulation capability and output robustness. The SC-based power converter, also known as a charge pump consisting of only semiconductor switches and capacitors, is a good one of the solutions to low-power DC-DC conversion. Unlike the traditional converter, the SC converter needs no magnetic element, e.g., inductor and transformer, so the SC converter always possesses light weight, small volume, and lower electromagnetic interference (EMI). Thus, such a SC-based converter is promising for VLSI fabrication, and many researchers/ manufactures pay more attention to development of SC converters realized on a chip by mixed analog VLSI technology.

In general, a charge pump SC converter is designed to obtain an output voltage higher than times the supply voltage or a reverse-polarity voltage. Such a step-up/reverse function is suitable to be applied to power-transistor driver [1], op-amp power supply [2], flash EEPROM [3-4], white light emitting diode (WLED) [5], and fluorescent lamp [6], etc. In fact, the idea of SC circuit has existed for nearly half a century. Brugler suggested SC voltage multiplier in 1971 [7], and then Lin and Chua presented topological generation and analysis of voltage multiplier [8]. Up to now, the various types of SC converters have been suggested for power conversion, and the most famous topologies of them are as follows: (i) Dickson charge pump [9-11], (ii) Ioinovici SC converter [12-15], and (iii) Makowski charge pump [19-22]. In 1976, Dickson charge pump was proposed in [9], and composed of a diode chain connected with two-phase clock inputs via pumping capacitors. By two-phase clock control, it can provide the fixed step-up voltage gain proportional to the stage number of pumping capacitors. Further, its detailed dynamic model and efficiency analysis are discussed in [10-11]. But, the drawback is that it has the fixed voltage gain and the larger fabrication area for the higher voltage gain. In 1993, Cheong, Chung, and Ioinovici suggested a new voltage-mode SC...
configuration, composed of two symmetry capacitor cells working complementarily [12]. And then, by using PWM technique, they proposed a step-up DC-DC converter in order to have the flexible voltage gain for output regulation [13]-[14]. In 1996, Chung and Ioinovici proposed a new current-mode SC scheme [15]. In fact, this new scheme is almost similar to [12], but the different point is to charge capacitors by a current source [15], not by a voltage source [12]. Such a current-mode scheme has the continuous current at source terminal, so the EMI problem can be improved. Following the same idea, Chang also proposed an integrated scheme of SC step-down/step-up DC-DC converter/DC-AC inverter [16-18]. However, Ioinovici SC converters still provide the step-up voltage gain just proportional to the number of pumping capacitors. So, it still requires the larger device area when the higher voltage gain is asked.

For the better voltage gain, Makowski suggested a multiplier charge pump composed of the two-phase cascaded voltage doublers in [19]. Via two-phase clock inputs for charge control, an n-stage Makowski charge pump can obtain the maximum boosting voltage gain limited by the \((n+1)\)th Fibonacci number. Its steady-state analysis, voltage loss and power loss are discussed in [20-21]. And further, in the two-phase SC converters, Makowski charge pump has been proved just to require the least number of pumping capacitors for some voltage gain given. So, Makowski charge pump just needs the smaller fabrication area. Following this idea, Starzyk proposed a new charge pump scheme, called multiphase voltage doubler (MPVD), and the most different point is to use multiphase clocks for charge control [22], not two-phase clock before. By such a multiphase control, the voltage gain can be achieved to increase up to \(2^n\) at most in the \(n\)-stage MPVD. So, for some voltage gain asked, the number of pumping capacitors in Starzyk is required fewer than that in Makowski. In other words, MPVD has the lower cost on fabrication area. Nevertheless, some improvement spaces still exist as follows. (i) Since the MPVD circuit scheme is fixed, the voltage conversion ratio is a constant value which is decided by the circuit parameters: MOSFET, capacitors, and supply voltage. However, for the different desired outputs/loading variations, the more flexible voltage gain is needed to enhance the output regulation capability. (ii) Since the source voltage is decreasing with the running time of batteries, or the source has the impure DC component due to the bad-quality batteries in portable electronic equipments, then lots of source noises occur. So, it is necessary to take care of output robustness against source disturbances. In this paper, the PWM control is adopted for the closed-loop output regulation and robustness. Besides, according to the desired output range, the voltage gain is changed automatically \((4x/3x/2x/1x)\) via the four-level control in order to improve the conversion efficiency, especially for the lower desired output. The main purpose of this paper is to propose a voltage-mode two-stage MPVD configuration via four-level PWM control for the flexible voltage gain and high-efficiency DC-DC step-up/down conversion/regulation.

2. Configuration of Four-Level PWM-Based MPVD:

Fig.1 shows a closed-loop configuration of two-stage MPVD with four-level PWM control, and it contains two major parts: “power part” and “control part”. The power part is shown in the upper half of Fig.1, called a voltage-mode two-stage MPVD converter, which is proposed and modified based on Starzyk charge pump [22]. This MPVD is basically composed of two cascaded voltage doublers in series connection between source and output terminals. For more details, it includes 2 pumping capacitors \(C_1, C_2\), 1 buffering and output capacitor \(C_3, C_o\), 8 MOSFET switches
$S_1, S_2, S_3, \ldots, S_8$, and 1 PWM switch $S_{PWM}$, where each capacitor has the same capacitance $C$ with equivalent series resistance (ESR) $r_C$ ($C_1 = C_2 = C_3 = C$), and similarly the output capacitor has capacitance $C_o$ with ESR $r_{Co}$, and MOSFETs $S_1, S_2, S_3, \ldots, S_8, S_{PWM}$ are operated as static switches with the on-state resistance $r_T$. Here, for the better conversion efficiency, the four-level control is added into the multiphase operation to change the voltage gain automatically (4x/3x/2x/1x) according to the range of the desired output. In other words, according to the different desired output range, the different MOSFET operations are scheduled and performed automatically so as to make the maximum output voltage $v_o$ be 4, 3, 2, or 1 times the source voltage $V_S$. Such a change on step-up voltage gain will be helpful to improve the conversion efficiency, especially for the low-voltage desired output.

First, let’s look at the basic operation for the 4x MPVD. Fig.2 shows its relevant theoretical waveforms in one PWM cycle $T_{PWM}$, which is defined as the inverse value of the PWM frequency $f_{PWM}$ ($T_{PWM} = 1/f_{PWM}$). Each one PWM cycle $T_{PWM}$ contains two states: ON/OFF state of $S_{PWM}$. The ON-state interval is denoted by $D \cdot T_{PWM}$, and the OFF-state interval is $(1-D) \cdot T_{PWM}$, where $D$ represents the duty cycle for PWM control ($0 \leq D \leq 1$). Here, to be easy for explanation, one PWM cycle $T_{PWM}$ contains 10 MPVD switching cycle $T_S$, which is the inverse of switching frequency $f_S$ for MPVD ($T_S = 1/f_S$). Actually, for the faster MPVD response to step-up conversion, it is feasible that $f_S$ is taken at 10 times or higher value of PWM frequency $f_{PWM}$. And then, each one MPVD cycle $T_S$ is divided into 4 small cycles denoted by Phase I, II, III, IV, with the small cycle value of $T$ ($T_S = 4T$). Now, let’s look at the Phase I–IV operations in one MPVD cycle $T_S$ within the ON-state interval of $D \cdot T_{PWM}$: (i) In Phase I, let $S_1, S_2, S_{PWM}$ turn on. Then, the Phase I topology is obtained as shown in Fig.3(a): $v_{C1}$ across $C_1$ is charged up to $V_S$, and buffering capacitor $C_3$ and output capacitor $C_o$ are discharged to supply the load $R_L$. (ii) In Phase II, let $S_3, S_4, S_5, S_6, S_{PWM}$ turn on. The Phase II topology is shown in Fig.3(b): $v_{C2}$ across $C_2$ is charged by the series connection with $V_S, v_{C1}$, and $C_3$ and $C_o$ are still discharged together to supply the load $R_L$. (iii) In Phase III, it repeats the Phase I operation. (iv) In Phase IV, let $S_3, S_4, S_7, S_8$, and $S_{PWM}$ turn on. The Phase IV topology is shown in Fig.3(c): $C_3$ and $C_o$ are charged simultaneously via the series connection with $V_S, v_{C1}$, and $v_{C2}$ to supply the load $R_L$. Next, let’s look at the Phase I–IV operations in one cycle $T_S$ within the OFF-state interval of $(1-D) \cdot T_{PWM}$. In fact, the Phase I–IV operations within the OFF-state interval are almost similar to the above but turning off $S_{PWM}$. So, the topologies for Phase I–IV within $(1-D) \cdot T_{PWM}$ are shown in Fig.4(a)–(c). For instance, the Phase IV operation within the OFF-state interval is to turn on $S_3, S_4, S_7,$ and $S_8$ only. So, the buffering capacitor $C_3$ is just charged by the series connection with $V_S, v_{C1}$, and $v_{C2}$. At this moment, only the output capacitor $C_o$ is discharged to supply the load $R_L$ as shown in Fig.4(c). From the above description, it is obvious that output $v_o$ can be regulated relative to how long the charging time $D \cdot T_{PWM}$ is, and maximum output voltage $v_o$ can be boosted up to 4 times source voltage $V_S$ at most theoretically in the 4x MPVD. Following the same idea, the MOSFET operations for the 3x/2x/1x MPVD can also be scheduled and listed in Table 1. This table shows the timing-control operations of MOSFETs for the four-level control (4x/3x/2x/1x).

Secondly, the control part: PWM controller is used as shown in the lower half of Fig.1, which is composed of low-pass filter (LPF), PWM block and phase generator. First, from the view of controller signal flow, the MPVD
feedback signal: output voltage \( v_o \) is sent into LPF for high-frequency noise rejection. Next, the filtered output \( v_o \) is compared with the desired output reference \( V_{ref} \) so as to produce the duty cycle \( D \) of MOSFET \( S_{PWM} \) via the PWM block. In this paper, by using the PWM control, the regulation capability of MPVD will be improved for different desired outputs/source or loading variations. In addition, a phase generator can be realized based on frequency divider to generate the MOSFET driver signals \( S_1 \sim S_8 \) for the four-level multiphase control as shown in Table 1. It results in the automatic change on the step-up voltage gain according to the range of the desired output, and then it will be helpful to obtain the better conversion efficiency, especially for the lower output voltage.

3. **Formulation of Four-Level PWM-Based MPVD:**

In this section, the state-space description of MPVD is derived for the four-level operation (4x/3x/2x/1x). Here, we start with the 4x MPVD formulation. Firstly, let’s look at Phase I-IV in one MPVD cycle \( T_S \) within the ON-state interval of \( D \cdot T_{PWM} \). In Phase I \( (t \in [t_0, t_1]) \), the operation is to let \( S_1, S_2, S_{PWM} \) turn on and the other MOSFETs be off, and then the topology is shown in Fig.3(a). According to this topology, the dynamic equation for Phase I within the ON-state interval can be described as

- **Phase I, III within** \( D \cdot T_{PWM} \):

\[
\begin{bmatrix}
\dot{v}_{C_1}(t) \\
\dot{v}_{C_2}(t) \\
\dot{v}_{C_3}(t) \\
\dot{v}_{C_4}(t)
\end{bmatrix} =
\begin{bmatrix}
\frac{-1}{R_{4x}C} & 0 & 0 & 0 \\
0 & \frac{-1}{\tau T C_o} & \frac{-1}{\tau T C_o} & \frac{-1}{\tau T C_o} \\
0 & \frac{-1}{\tau T C_o} & \frac{-1}{\tau T C_o} & \frac{-1}{\tau T C_o} \\
0 & \frac{-1}{\tau T C_o} & \frac{-1}{\tau T C_o} & \frac{-1}{\tau T C_o}
\end{bmatrix}
\begin{bmatrix}
v_{C_1}(t) \\
v_{C_2}(t) \\
v_{C_3}(t) \\
v_{C_4}(t)
\end{bmatrix} +
\begin{bmatrix}
\frac{1}{R_{4x}C} \\
0 \\
0 \\
0
\end{bmatrix} \cdot v_S,
\]

(1a)

\[
\begin{bmatrix}
v_o(t) \\
i_S(t)
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 & 1 \\
0 & 0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
v_{C_1}(t) \\
v_{C_2}(t) \\
v_{C_3}(t) \\
v_{C_4}(t)
\end{bmatrix} +
\begin{bmatrix}
0 \\
\frac{1}{R_{4x}}
\end{bmatrix} \cdot v_S,
\]

(1b)

where the parasitic resistance \( R_{4x} = 2 \cdot \tau T + r_C \) for the 4x MPVD, and \( v_o(t), i_S(t) \) represent the output voltage and the current at supply source terminal, respectively. In Phase II \( (t \in [t_1, t_2]) \), the operation is to turn on \( S_3, S_4, S_5, S_6, S_{PWM} \), and the topology is shown in Fig.3(b). Based on this topology, the dynamic equation for Phase II within the ON-state interval is described as

- **Phase II within** \( D \cdot T_{PWM} \):

\[
\begin{bmatrix}
\dot{v}_{C_1}(t) \\
\dot{v}_{C_2}(t) \\
\dot{v}_{C_3}(t) \\
\dot{v}_{C_4}(t)
\end{bmatrix} =
\begin{bmatrix}
\frac{-1}{2R_{4x}C} & \frac{1}{2R_{4x}C} & 0 & 0 \\
\frac{1}{2R_{4x}C} & \frac{-1}{2R_{4x}C} & \frac{-1}{\tau T C_o} & \frac{-1}{\tau T C_o} \\
0 & 0 & \frac{-1}{\tau T C_o} & \frac{-1}{\tau T C_o} \\
0 & 0 & \frac{-1}{\tau T C_o} & \frac{-1}{\tau T C_o}
\end{bmatrix}
\begin{bmatrix}
v_{C_1}(t) \\
v_{C_2}(t) \\
v_{C_3}(t) \\
v_{C_4}(t)
\end{bmatrix} +
\begin{bmatrix}
\frac{-1}{2R_{4x}C} \\
\frac{1}{2R_{4x}C} \\
0 \\
0
\end{bmatrix} \cdot v_S,
\]

(2a)

\[
\begin{bmatrix}
v_o(t) \\
i_S(t)
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 & 1 \\
\frac{1}{2R_{4x}} & \frac{-1}{2R_{4x}} & 0 & 0
\end{bmatrix}
\begin{bmatrix}
v_{C_1}(t) \\
v_{C_2}(t) \\
v_{C_3}(t) \\
v_{C_4}(t)
\end{bmatrix} +
\begin{bmatrix}
0 \\
\frac{1}{2R_{4x}}
\end{bmatrix} \cdot v_S,
\]

(2b)

Next, Phase III \( (t \in [t_2, t_3]) \) repeats the Phase I operation. So, the topologies of Phase I and III are the same as shown
in Fig. 3(a), and the dynamic equation for Phase III is completely identical to (1). In Phase IV \((t \in [t_3, t_4])\), let \(S_3, S_4, S_7, S_8\), and \(S_{PWM}\) turn on. The Phase IV topology is shown in Fig.3(c): \(C_3\) and \(C_o\) are charged simultaneously via the series connection with \(V_S\), \(v_{C1}\), and \(v_{C2}\) to supply the load \(R_L\). So, the dynamic equation for Phase IV within the ON-state interval is derived as

**Phase IV within \(D \cdot T_{PWM}\):**

\[
\begin{bmatrix}
\frac{v_{C1}(t)}{v_{C2}(t)} \\
\frac{v_{C3}(t)}{v_{C0}(t)}
\end{bmatrix}
= \begin{bmatrix}
-\frac{1}{2R_{4x}} & -\frac{1}{2R_{4x}} \\
-\frac{2R_{4x}}{C} & -\frac{2R_{4x}}{C} \\
0 & 0 \\
0 & 0
\end{bmatrix}
\begin{bmatrix}
v_{C1}(t) \\
v_{C2}(t) \\
v_{C3}(t) \\
v_{C0}(t)
\end{bmatrix}
+ \begin{bmatrix}
\frac{1}{2R_{4x}} \\
\frac{1}{2R_{4x}} \\
\frac{1}{2R_{4x}} \\
\frac{1}{2R_{4x}}
\end{bmatrix}
\cdot V_S,
\]

Based on (1)–(3), the averaged dynamic equation of MPVD within the ON-state interval can be computed by using state-space averaging technique, \([(1)+(2)+(1)+(3)]/4\), to be formulated as:

\[
\begin{bmatrix}
\frac{v_{C1}(t)}{v_{C2}(t)} \\
\frac{v_{C3}(t)}{v_{C0}(t)}
\end{bmatrix}
= \begin{bmatrix}
-\frac{3}{4R_{4x}} & 0 \\
0 & -\frac{1}{4R_{4x}} \\
\frac{1}{8R_{4x}} & \frac{1}{8R_{4x}} \\
0 & 0
\end{bmatrix}
\begin{bmatrix}
v_{C1}(t) \\
v_{C2}(t) \\
v_{C3}(t) \\
v_{C0}(t)
\end{bmatrix}
+ \begin{bmatrix}
\frac{1}{4R_{4x}} \\
\frac{1}{4R_{4x}} \\
\frac{1}{8R_{4x}} \\
\frac{1}{8R_{4x}}
\end{bmatrix}
\cdot V_S,
\]

Secondly, let’s look at Phase I–IV within the OFF-state interval of \((1-D) \cdot T_{PWM}\). In fact, the Phase I–IV operations within the OFF-state interval of \((1-D) \cdot T_{PWM}\) are almost similar to the operations within the ON-state interval as above, but the difference is to turn off \(S_{PWM}\). So, the topologies for Phase I–IV within the OFF-state interval can be obtained as shown in Fig.4(a)–(c), and then, the dynamic equations for Phase I–IV within the OFF-state interval of \((1-D) \cdot T_{PWM}\) can be derived as shown in (5)–(7), respectively.

**Phase I, III within \((1-D) \cdot T_{PWM}\):**

\[
\begin{bmatrix}
\frac{v_{C1}(t)}{v_{C2}(t)} \\
\frac{v_{C3}(t)}{v_{C0}(t)}
\end{bmatrix}
= \begin{bmatrix}
0 & 0 \\
0 & 0 \\
0 & 0 \\
0 & 0
\end{bmatrix}
\begin{bmatrix}
v_{C1}(t) \\
v_{C2}(t) \\
v_{C3}(t) \\
v_{C0}(t)
\end{bmatrix}
+ \begin{bmatrix}
\frac{1}{R_{4x}} \\
0 \\
0 \\
0
\end{bmatrix}
\cdot V_S,
\]

\[
\begin{bmatrix}
\frac{v_{o}(t)}{i_{S}(t)}
\end{bmatrix}
= \begin{bmatrix}
0 & 0 & 0 \\
0 & 0 & 0 \\
0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
v_{C1}(t) \\
v_{C2}(t) \\
v_{C3}(t) \\
v_{C0}(t)
\end{bmatrix}
+ \begin{bmatrix}
0 \\
0 \\
0
\end{bmatrix}
\cdot V_S,
\]
Phase II within $(1-D) \cdot T_{PWM}$:

$$
\begin{bmatrix}
\begin{bmatrix}
\frac{v_{C_1}(t)}{v_{C_2}(t)}
\end{bmatrix}
+ \begin{bmatrix}
\frac{1}{2R_4x}C
\end{bmatrix}
\end{bmatrix}
\begin{bmatrix}
\frac{v_{C_1}(t)}{v_{C_2}(t)}
\end{bmatrix}
= \begin{bmatrix}
0
0
0
0
\end{bmatrix}
+ \begin{bmatrix}
\frac{1}{2R_4x}C
\end{bmatrix}
\begin{bmatrix}
0
0
0
0
\end{bmatrix}
\cdot V_S,
$$

(6a)

Phase IV within $(1-D) \cdot T_{PWM}$:

$$
\begin{bmatrix}
\begin{bmatrix}
\frac{v_{C_1}(t)}{v_{C_2}(t)}
\end{bmatrix}
+ \begin{bmatrix}
\frac{1}{2R_4x}C
\end{bmatrix}
\end{bmatrix}
\begin{bmatrix}
\frac{v_{C_1}(t)}{v_{C_2}(t)}
\end{bmatrix}
= \begin{bmatrix}
0
0
0
0
\end{bmatrix}
+ \begin{bmatrix}
\frac{1}{2R_4x}C
\end{bmatrix}
\begin{bmatrix}
0
0
0
0
\end{bmatrix}
\cdot V_S,
$$

(6b)

Based on (5)–(7), the averaged dynamic equation of MPVD within the OFF-state interval can also be computed by using averaging technique, $[(5) + (6) + (5) + (7)]/4$ as shown in (8).

$$
\begin{bmatrix}
\begin{bmatrix}
\frac{v_{C_1}(t)}{v_{C_2}(t)}
\end{bmatrix}
+ \begin{bmatrix}
\frac{1}{2R_4x}C
\end{bmatrix}
\end{bmatrix}
\begin{bmatrix}
\frac{v_{C_1}(t)}{v_{C_2}(t)}
\end{bmatrix}
= \begin{bmatrix}
0
0
0
0
\end{bmatrix}
+ \begin{bmatrix}
\frac{1}{2R_4x}C
\end{bmatrix}
\begin{bmatrix}
0
0
0
0
\end{bmatrix}
\cdot V_S,
$$

(7a)

Finally, let’s take the weighted average of (4) and (8), $[(4) \times D \cdot T_{PWM} + (8) \times (1-D) \cdot T_{PWM}]/T_{PWM}$, and then the state-space averaged description of the 4x MPVD can be derived as

$$
x'(t) = A_{4x} \cdot x(t) + B_{4x} \cdot u(t),
$$

(9a)

$$
y(t) = C_{4x} \cdot x(t) + D_{4x} \cdot u(t),
$$

(9b)

where

$$
x(t) = \begin{bmatrix} v_{C_1}(t) & v_{C_2}(t) & v_{C_3}(t) & v_{C_4}(t) \end{bmatrix}^T,
$$

(10a)

$$
u(t) = \begin{bmatrix} V_S \end{bmatrix}^T,
$$

(10b)

$$
y(t) = \begin{bmatrix} v_o(t) & i_S(t) \end{bmatrix}^T,
$$

(10c)
$$A_{4x} = \begin{bmatrix} \frac{3}{4R_{4x}C} & 0 & \frac{1}{8R_{4x}C} & 0 \\ 0 & -\frac{1}{4R_{4x}C} & \frac{1}{8R_{4x}C} & 0 \\ \frac{1}{8R_{4x}C} & \frac{1}{8R_{4x}C} & -\frac{D}{\gamma T C} & \frac{D}{\gamma T C} \\ 0 & 0 & -\frac{D}{\gamma T C} & \frac{1}{R_{L}C_{o}} \end{bmatrix}, \quad B_{4x} = \begin{bmatrix} \frac{1}{4R_{4x}C} \\ 0 \\ 0 \\ \frac{1}{8R_{4x}C} \end{bmatrix},$$

$$C_{4x} = \begin{bmatrix} 0 & 0 & 0 & 1 \\ -\frac{1}{4R_{4x}} & 0 & -\frac{1}{8R_{4x}} & 0 \end{bmatrix}, \quad D_{4x} = \begin{bmatrix} 0 \\ \frac{3}{4R_{4x}} \end{bmatrix} \cdot (R_{4x} = 2 \cdot \gamma T + \gamma C)$$

Similarly, by using the same derivation, based on the four-level control in Table 1, the state-space averaged descriptions of the 3x/2x/1x MPVD can be formulated as shown in (11)-(13), respectively. The theoretical analysis and control design will become much easier due to the averaged MPVD formulations.

$$\begin{align*}
\begin{bmatrix} v_{C_1}(t) \\ v_{C_2}(t) \\ v_{C_3}(t) \\ v_{C_0}(t) \end{bmatrix} &= \begin{bmatrix} \frac{3}{4R_{3x}C} & 0 & \frac{1}{8R_{3x}C} & 0 \\ 0 & -\frac{1}{4R_{3x}C} & \frac{1}{8R_{3x}C} & 0 \\ \frac{1}{8R_{3x}C} & \frac{1}{8R_{3x}C} & -\frac{D}{\gamma T C} & \frac{D}{\gamma T C} \\ 0 & 0 & -\frac{D}{\gamma T C} & \frac{1}{R_{L}C_{o}} \end{bmatrix} \cdot \begin{bmatrix} v_{C_1}(t) \\ v_{C_2}(t) \\ v_{C_3}(t) \\ v_{C_0}(t) \end{bmatrix} \cdot V_S \cdot (R_{3x} = 2 \cdot \gamma T + \gamma C) \quad \text{[3x MPVD]} \\
\begin{bmatrix} v_{C_1}(t) \\ v_{C_2}(t) \\ v_{C_3}(t) \\ v_{C_0}(t) \end{bmatrix} &= \begin{bmatrix} 0 \\ 0 \\ \frac{1}{4R_{2x}} \end{bmatrix} \cdot \begin{bmatrix} 0 \\ 0 \\ \frac{1}{4R_{2x}} \end{bmatrix} \cdot \begin{bmatrix} v_{C_1}(t) \\ v_{C_2}(t) \\ v_{C_3}(t) \\ v_{C_0}(t) \end{bmatrix} \cdot \frac{1}{R_{2x}} \cdot V_S \cdot (R_{2x} = 4 \cdot \gamma T + \gamma C) \quad \text{[2x MPVD]} \\
\begin{bmatrix} v_{C_1}(t) \\ v_{C_2}(t) \\ v_{C_3}(t) \\ v_{C_0}(t) \end{bmatrix} &= \begin{bmatrix} 0 \\ 0 \\ \frac{1}{4R_{1x}} \end{bmatrix} \cdot \begin{bmatrix} 0 \\ 0 \\ \frac{1}{4R_{1x}} \end{bmatrix} \cdot \begin{bmatrix} v_{C_1}(t) \\ v_{C_2}(t) \\ v_{C_3}(t) \\ v_{C_0}(t) \end{bmatrix} \cdot \frac{1}{R_{1x}} \cdot V_S \cdot (R_{1x} = 4 \cdot \gamma T) \quad \text{[1x MPVD]}
\end{align*}$$

4. Analysis and Design of Four-Level PWM-Based MPVD:

4.1 Steady-state analysis and voltage conversion ratio:

Here, both steady-state analysis and voltage conversion ratio will be discussed. First, let’s look at the steady-state
analysis of the 4x MPVD. For steady-state analysis, by substituting $x'=0$ of (9a), the steady-state output voltage $V_o$, output current $I_o$, and source-terminal current $I_S$ can be derived as

$$V_o = (-C_{4x,1} \cdot A_{4x,1}^{-1} \cdot B_{4x} + D_{4x,1}) \cdot u = \frac{D \cdot 4 \cdot V_S}{D \cdot (1 + 24 \cdot R_{4x}) + \frac{r_T}{R_L}}, \quad I_o = \frac{V_o}{R_L},$$

(14a,b)

$$I_S = (-C_{4x,2} \cdot A_{4x,2}^{-1} \cdot B_{4x} + D_{4x,2}) \cdot u = \frac{D \cdot 16 \cdot V_S}{D \cdot (R_L + 24 \cdot R_{4x}) + \frac{r_T}{R_L}} = 4 \cdot \frac{V_o}{R_L} = 4 \cdot I_o,$$

(14c)

where $C_{4x,1}/C_{4x,2}$ are the matrices which are the 1st/2nd row of $C_{4x}$ ($D_{4x}$), respectively. From (14a), it is obvious that the steady-state output voltage $V_o$ can be regulated via the control of duty cycle $D$, and then the DC-DC voltage conversion ratio $M_{4x}$ for the 4x MPVD can be suggested as

$$M_{4x} = \frac{V_o}{V_S} = \frac{4 \cdot D}{D \cdot (1 + 24 \cdot R_{4x}) + \frac{r_T}{R_L}}.$$  

(15)

If duty cycle $D = 0$, then the voltage conversion ratio $M_{4x}$ is 0. If $D = 1$, the maximum value of $M_{4x}$ occurs, and it is truly close to 4 when $R_L >> r_T, r_C$. In other words, $V_o$ is boosted up to 4 times the voltage of source $V_S$ at most in the 4x MPVD. For nominal conditions, the maximum attainable output $V_o$ is $4 \cdot V_S$, voltage drops in the charging and discharging circuits. For the better conversion ratio, the value of load $R_L$ applied is supposed to be much larger than the value of parasitic $r_T, r_C$. In fact, load $R_L$ is about in $\Omega$-level, and $r_T, r_C$ is about in $\text{m}\Omega$-level. Following the same process, the steady-state analysis and the voltage conversion ratio for the $3x/2x/1x$ MPVD can be derived as shown in (16a)–(18), respectively.

$$V_o = \frac{D \cdot 3 \cdot V_S}{D \cdot (1 + \frac{15 \cdot R_{3x}}{R_L}) + \frac{r_T}{R_L}}, \quad M_{3x} = \frac{V_o}{V_S} = \frac{3 \cdot D}{D \cdot (1 + \frac{15 \cdot R_{3x}}{R_L}) + \frac{r_T}{R_L}}.$$  

[3x MPVD]  

(16a,b)

$$V_o = \frac{D \cdot 2 \cdot V_S}{D \cdot (1 + \frac{4 \cdot R_{2x}}{R_L}) + \frac{r_T}{R_L}}, \quad M_{2x} = \frac{V_o}{V_S} = \frac{2 \cdot D}{D \cdot (1 + \frac{4 \cdot R_{2x}}{R_L}) + \frac{r_T}{R_L}}.$$  

[2x MPVD]

(17a,b)

$$V_o = \frac{D \cdot 1 \cdot V_S}{D \cdot (1 + \frac{1 \cdot R_{1x}}{R_L}) + \frac{r_T}{R_L}}, \quad M_{1x} = \frac{V_o}{V_S} = \frac{1 \cdot D}{D \cdot (1 + \frac{1 \cdot R_{1x}}{R_L}) + \frac{r_T}{R_L}}.$$  

[1x MPVD]

(18a,b)

### 4.2 Power conversion efficiency:

Based on theoretical analysis of (14), its steady-state input/output power can be computed as:

$$P_i = V_S \cdot I_S = V_S \cdot 4 \cdot I_o, \quad P_o = V_o \cdot I_o.$$  

(19a,b)

Thus, by combining (19) and (15), the power conversion efficiency of the 4x MPVD is derived as

$$\eta_{4x} = \frac{P_o}{P_i} = \frac{V_o \cdot I_o}{V_S \cdot 4 \cdot I_o} = \frac{1}{4} \frac{V_o}{V_S} = \frac{M_{4x}}{4} = \frac{D}{D \cdot (1 + 24 \cdot R_{4x}) + \frac{r_T}{R_L}}, \quad 0 \leq V_o \leq 4 \cdot V_S.$$  

(20)

By the same process, the power conversion efficiency for the other voltage gains can be derived as follows:

$$\eta_{3x} = \frac{P_o}{P_i} = \frac{V_o \cdot I_o}{V_S \cdot 3 \cdot I_o} = \frac{1}{3} \frac{V_o}{V_S} = \frac{M_{3x}}{3} = \frac{D}{D \cdot (1 + \frac{15 \cdot R_{3x}}{R_L}) + \frac{r_T}{R_L}}, \quad 0 \leq V_o \leq 3 \cdot V_S.$$  

[3x MPVD]  

(21a)

$$\eta_{2x} = \frac{P_o}{P_i} = \frac{V_o \cdot I_o}{V_S \cdot 2 \cdot I_o} = \frac{1}{2} \frac{V_o}{V_S} = \frac{M_{2x}}{2} = \frac{D}{D \cdot (1 + \frac{4 \cdot R_{2x}}{R_L}) + \frac{r_T}{R_L}}, \quad 0 \leq V_o \leq 2 \cdot V_S.$$  

[2x MPVD]  

(21b)
\[ \eta_{1x} = \frac{P_0}{P_1} = \frac{V_o \cdot I_o}{V_S \cdot I_0} = \frac{1}{V_S} \frac{V_o}{1} = \frac{M_{1x} \cdot D}{(1 + R_{1x}) + \frac{R_F}{R_L}}. \quad 0 \leq V_o \leq 1 \cdot V_S \quad [1 \times \text{MPVD}] \]  

(21c)

From (20), it is obvious that efficiency \( \eta_{4x} \) is sure to increase with adding \( M_{4x} \). So, for the better efficiency, it is good to choose the desired output \( V_o \) as close to \( 4 \cdot V_S \) as possible. However, if the operating \( M_{4x} \) is much smaller than 4, i.e., \( V_o << 4 \cdot V_S \), then the efficiency will be quite bad. The situation often appears in the low-voltage output required. Here, to improve conversion efficiency, the four-level control design is added and employed to change the voltage gain automatically (4x/3x/2x/1x) according to the desired output range. In other words, the four-level output of \( m \cdot V_S \) (\( m = 1, 2, 3, \) or \( 4 \)) can be changed automatically via the four-level control in order to fit the desired output \( V_o \) as much as possible. For example, source \( V_S \) is \( 3.6 \) \( V \), and the maximum output voltage can be boosted up to \( 14.4 \) \( V \) via the 4x MPVD theoretically. But, the desired output \( V_o \) is just asked to be \( 7 \) \( V \) now. If the 4x MPVD is still employed, it is obtained from (20) that the best efficiency will not be higher than \( 48.6 \) \%. For the 3x MPVD, the best efficiency is estimated from (21a) to be \( 64.8 \) \% at most. But, if the 2x MPVD is adopted here, then the best efficiency is improved up to about \( 97.2 \) \% from (21b). The reason is that \( 2 \cdot V_S \) is close to the desired output of \( 7 \) \( V \) most right now. Therefore, the four-level control is able to improve the power conversion efficiency, especially for the low-voltage output required.

### 4.3 Output ripple and capacitance selection:

According to Fig.2, output voltage \( v_o \) across load \( R_L \) is decaying exponentially from \( V_{0,\text{max}} \) to \( V_{0,\text{min}} \) during the OFF-state time interval of \( (1 - D) \cdot T_{PWM} \) cyclically, and then \( v_o \) can be modeled as:

\[ v_o(t) = V_{0,\text{max}} \cdot e^{-t/\tau}, \quad 0 \leq t \leq (1 - D) \cdot T_{PWM}. \]

(22)

where the maximum/minimum output is denoted by \( V_{0,\text{max}} / V_{0,\text{min}} \) in the OFF-state interval, and formulated by \( V_{0,\text{max}} = v_o(0) \) and \( V_{0,\text{min}} = v_o((1 - D) \cdot T_{PWM}) = V_{0,\text{max}} \cdot e^{-(1 - D)\cdot T_{PWM}/\tau} \), where the discharging time constant \( \tau = R_L \cdot C_o \). So, the ripple variation of output voltage can be defined as:

\[ \Delta v_o = V_{0,\text{max}} - V_{0,\text{min}} = V_{0,\text{max}} \cdot [1 - e^{-(1 - D) \cdot T_{PWM} / \tau}]. \]

(23)

Next, the averaged output voltage can be calculated by (24) as:

\[ V_o = \frac{1}{(1 - D) \cdot T_{PWM}} \int_0^{(1 - D) \cdot T_{PWM}} v_o(t) \, dt = \frac{1}{1 - D} \cdot f_{PWM} \cdot \tau \cdot \Delta v_o. \]

(24)

By combining (23) and (24), the output ripple percentage can be presented as:

\[ r_p = \frac{\Delta v_o}{V_o} \times 100\% = \frac{1 - D}{f_{PWM} \cdot \tau} = \frac{1 - D}{f_{PWM} \cdot R_L \cdot C_o}. \]

(25)

Here, it is found that the ripple percentage \( r_p \) is worse while the load is heavier, but it can be improved by increasing PWM frequency \( f_{PWM} \) or output capacitor \( C_o \). Obviously, when the MPVD is unloaded \( (R_L \rightarrow \infty) \), \( r_p \) is almost zero. For a desired ripple percentage \( r_{\bar{p}} \) and a specified PWM frequency \( f_{PWM} \), based on (25), the minimum output capacitor can be estimated as

\[ C_o \geq C_{o,\text{min}} = \frac{1 - D}{f_{PWM} \cdot R_L \cdot r_{\bar{p}}}. \]

(26)
4.4 Stability of four-level MPVD:

In this section, the open-loop stability of MPVD is discussed. First, let’s talk about the stability of the 4x MPVD. Here, its relative system matrix \( A_{4x} \) of (10d) is divided into 4 sub-matrix \( A_{11} \sim A_{22} \), and then \( A_{4x} \) can be decomposed as shown in (27a), where the diagonal sub-matrix \( \Delta_{4x} \) is computed as shown in (27b). Obviously, the system stability depends on the poles of \( A_{11} \) and \( \Delta_{4x} \).

\[
A_{4x} = \begin{bmatrix}
\frac{3}{4R_{4x}C} & 0 & \frac{1}{8R_{4x}C} & 0 \\
0 & \frac{1}{4R_{4x}C} & \frac{1}{8R_{4x}C} & \frac{D}{r_{T}C} \\
\frac{1}{8R_{4x}C} & \frac{1}{8R_{4x}C} & -\frac{D}{r_{T}C} & \frac{D}{r_{T}C} \\
0 & 0 & \frac{1}{r_{T}C_o} & -\frac{1}{r_{T}C_o}
\end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix}
\]

\( \Delta_{4x} = A_{22} - A_{21} \cdot A_{11}^{-1} \cdot A_{12} \)

\[
= \left( -\frac{D}{r_{T}C_o} - \frac{1}{R_{L}C_o} \right) \begin{bmatrix} I & 0 \\ A_{11} & 0 \\ A_{4x} & 0 \end{bmatrix} \begin{bmatrix} \frac{3}{4R_{4x}C} & 0 & \frac{1}{8R_{4x}C} & 0 \\ 0 & \frac{1}{4R_{4x}C} & \frac{1}{8R_{4x}C} & \frac{D}{r_{T}C} \\ \frac{1}{8R_{4x}C} & \frac{1}{8R_{4x}C} & -\frac{D}{r_{T}C} & \frac{D}{r_{T}C} \\ 0 & 0 & \frac{1}{r_{T}C_o} & -\frac{1}{r_{T}C_o} \end{bmatrix}^{-1} \begin{bmatrix} I \\ 0 \\ 0 \\ D \end{bmatrix}
\]

As above description for the better efficiency, the value of load \( R_{L} \) is supposed to be much larger than the value of parasitic \( r_{T}, r_{C} \) (\( R_{L} >> r_{T}, r_{C} \)). In addition, according to (26), the value of output capacitor \( C_{o} \) would be chosen larger for the better output ripple, even 10 times greater than the value of pumping capacitor \( C \) in general. So, the value \( R_{L}C_{o} \) in \( \Delta_{4x} \) is much larger than \( R_{4x}C \) in \( A_{11} \) (\( R_{L}C_{o} >> R_{4x}C \)). Then, it is easy to conclude that \( \Delta_{4x} \) dominates the stability of the 4x MPVD, and the system’s dominant pole of the open-loop 4x MPVD is \( \Delta_{4x} \) as shown in (27b). Obviously, this 4x MPVD is locally stable because the dominant pole \( \Delta_{4x} \) is located in the left half of s-plane no matter what the duty cycle \( D \) is set on (0 ≤ 0 ≤ 1). That almost ensures the global stability of voltage-mode MPVD. By the same decomposition as above, the dominant poles for the other voltage gains can be derived as follows:

\[
\Delta_{3x} = \left[ \frac{D}{(r_{T} + 15 \cdot D \cdot R_{4x}) \cdot C_{o}} + \frac{1}{R_{L}C_{o}} \right], \quad [3x \ MPVD]
\]

\[
\Delta_{2x} = \left[ \frac{D}{(r_{T} + 4 \cdot D \cdot R_{4x}) \cdot C_{o}} + \frac{1}{R_{L}C_{o}} \right], \quad [2x \ MPVD]
\]

\[
\Delta_{1x} = \left[ \frac{D}{(r_{T} + 1 \cdot D \cdot R_{4x}) \cdot C_{o}} + \frac{1}{R_{L}C_{o}} \right], \quad [1x \ MPVD]
\]

Similarly, these dominant poles are also all located in the left half of s-plane. Thus, it is one of advantages that this MPVD scheme has an inherent good stability.
4-5. PWM control of four-level MPVD:

In this section, let’s talk about the PWM control design for MPVD. This PWM controller is shown in the lower half of Fig.1, including LPF, PWM block, and phase generator. From the view of controller signal flow, the feedback signal: \( v_o \) is sent into LPF for high-frequency noise rejection. And then, the filtered output \( v_o \) is compared with the desired \( V_{\text{ref}} \) so as to produce the duty cycle \( D \) via the PWM block. The main goal of PWM controller is to let output \( v_o \) follow the desired \( V_{\text{ref}} \) by adjusting the duty cycle \( D \), and the output regulation capability is enhanced for the different desired outputs/source or loading variations. Here, the four-level PWM controller design can be treated as a simple low-pass proportional controller design (PI controller) as shown in Fig.5, and it is able to compensate the dynamic error between output voltage and desired reference, even for the compensation of rise or setting time. In this controller, there are two parameters including the cut-off frequency \( w_L \) and the proportional gain \( K_P \), where \( K_P \) is designed for the dynamic error compensation, and \( w_L \) is set for the possible high-frequency noise rejection. Now, let’s look at the proportional gain design. We assume that the 4x MPVD is operating around one operating point of duty cycle \( D_o \) for some desired reference \( V_{\text{ref}} \). In other words, the steady-state output \( v_o \) is following and equal to the desired reference \( V_{\text{ref}} \) under the duty cycle \( D_o \) right now. So, based on (14a), the relationship on this static operating point is formed as shown in (29a), and then by arranging (29a), the operating duty cycle \( D_o \) is shown in (29b).

\[
V_o = V_{\text{ref}} = \frac{D_o \cdot 4V_S}{D_o \left(1 + \frac{24R_{4x}}{R_L}\right) + \frac{r_T}{R_L}}, \quad \text{for } D = D_o. \tag{29a}
\]

\[
D_o = \frac{r_T}{\left(\frac{V_{\text{ref}}}{4V_S} - 1\right) \cdot R_L - 24 \cdot R_{4x}}. \tag{29b}
\]

When a small duty-cycle variation \( d \) occurs, the output voltage also has the small change \( \bar{v}_o \) as:

\[
V_o + \bar{v}_o = \frac{(D_o + d) \cdot 4V_S}{(D_o + d) \left(1 + \frac{24R_{4x}}{R_L}\right) + \frac{r_T}{R_L}}, \quad \text{for } D = D_o + d. \tag{30}
\]

By subtracting (29a) from (30), we have

\[
\bar{v}_o = \frac{(D_o + d) \cdot 4V_S}{(D_o + d) \left(1 + \frac{24R_{4x}}{R_L}\right) + \frac{r_T}{R_L}} - \frac{D_o \cdot 4V_S}{D_o \left(1 + \frac{24R_{4x}}{R_L}\right) + \frac{r_T}{R_L}} = \frac{4V_S \cdot \frac{r_T}{R_L} \cdot d}{D_o \left(1 + \frac{24R_{4x}}{R_L}\right) + \frac{r_T}{R_L}}.
\]

\[
\bar{v}_o \approx \frac{4V_S \cdot \frac{r_T}{R_L} \cdot d}{\left[D_o \left(1 + \frac{24R_{4x}}{R_L}\right) + \frac{r_T}{R_L}\right]^2}.
\]

Thus, by combining (29b) and (31), the small-signal output voltage \( \bar{v}_o \) around \( D_o \) can be rewritten as:

\[
\bar{v}_o = \frac{V_{\text{ref}} \cdot \frac{r_T}{R_L} \cdot d}{4V_S \cdot D_o^2 \cdot R_L}. \tag{32}
\]
It is obvious that the small-signal output voltage $\tilde{v}_o$ is regulated linearly by the duty cycle variation $d$. So, by combining the dominant pole $\Delta_{4x}$ of (27b), the small-signal output voltage $\tilde{v}_o$ can be written with one-order approximated transfer function of small-signal duty cycle $d$ as shown in (33).

$$v_o(s) = \tilde{v}_o \cdot d(s) = \frac{V_{\text{ref}}^2 \cdot r_T}{4V_S \cdot D_o^2 \cdot R_L} \cdot \frac{1}{\tau_{4x} \cdot s + 1} \cdot d(s), \quad (33)$$

where

$$\tau_{4x} = \frac{1}{\Delta_{4x} / D_o} = \left(\frac{D_o}{(r_T + D_o \cdot 24R_{4x}) \cdot C_o + R_L \cdot C_o}\right)^{-1} = C_o \cdot \left(\frac{R_L}{(24R_{4x} + \frac{r_T}{D_o})}\right). \quad (34)$$

$\tau_{4x}$ represents the small-signal open-loop time constant of the 4x MPVD. Next, according to (33), around this operating point $D_o$, a small-signal closed-loop diagram of the 4x MPVD can be suggested by combining PWM control as shown in Fig.6. In this figure, a PWM-based output feedback is applied ($d = -K_P \cdot v_o$) for dynamic output regulation, and then the small-signal closed-loop characteristic equation of the 4x MPVD can be derived as:

$$\Delta_{\text{pwm}}(s) = \tau_{4x} \cdot s + 1 + K_P \cdot \frac{V_{\text{ref}}^2 \cdot r_T}{4V_S \cdot D_o^2 \cdot R_L} = 0. \quad (35)$$

Thus, we rewrite (35) into (36), and then the small-signal closed-loop time constant of the 4x MPVD is obtained and denoted by $\tau_{4x,\text{pwm}}$ as shown in (37).

$$\Delta_{\text{pwm}}(s) = \tau_{4x,\text{pwm}} \cdot s + 1 = 0, \quad (36)$$

where

$$\tau_{4x,\text{pwm}} = \frac{\tau_{4x}}{1 + K_P \cdot \frac{V_{\text{ref}}^2 \cdot r_T}{4V_S \cdot D_o^2 \cdot R_L}}. \quad (37)$$

In general, the closed-loop setting time $t_{S,\text{pwm}}$ can be defined as three times values of time constant $\tau_{4x,\text{pwm}}$, and further, $t_{S,\text{pwm}}$ is required shorter than some desired setting time $\tilde{t}_S$ given, and then it is shown as:

$$t_{S,\text{pwm}} = 3 \cdot \tau_{4x,\text{pwm}} < \tilde{t}_S. \quad (38)$$

By substituting (37) into (38), we can obtain

$$K_P > \frac{4V_S \cdot D_o^2 \cdot R_L}{V_{\text{ref}}^2 \cdot r_T} \cdot \left(\frac{3\tau_{4x}}{\tilde{t}_S} - 1\right). \quad (39)$$

Finally, by combining (29b), (34), and (39), the proportional gain $K_P$ can be derived and designed as

$$K_P > \frac{r_T C_o}{4V_S - V_{\text{ref}}} \cdot \left(\frac{3}{\tilde{t}_S} - \frac{1}{\tau_{4x}} \cdot \frac{1}{\frac{R_L}{24R_{4x}} \cdot \left(\frac{1}{4V_S - V_{\text{ref}}} \cdot \frac{24R_{4x}}{R_L}\right)^2}\right). \quad (40)$$

Based on the gain $K_P$ of (40), it is achieved that $t_S$ would be shorter than the desired $\tilde{t}_S$ for the better transient response. By the same process as above, the proportional gain for the other voltage gains can also be derived as shown in (41a)-(41c), respectively. From the results, it is obvious that the larger gain $K_P$ is needed as the desired setting time $\tilde{t}_S$ is required shorter.
\[ K_P > \frac{r_f C_o}{3V_S - V_{ref}} \frac{3}{l_S} - \frac{1}{\tau_{3x}} \left( 1 - \frac{V_{ref}}{3V_S - V_{ref}} \frac{15R_{3x}}{R_L} \right)^2, \quad [3x \text{ MPVD}] \]  

\[ K_P > \frac{r_f C_o}{2V_S - V_{ref}} \frac{3}{l_S} - \frac{1}{\tau_{2x}} \left( 1 - \frac{V_{ref}}{2V_S - V_{ref}} \frac{4R_{2x}}{R_L} \right)^2, \quad [2x \text{ MPVD}] \]  

\[ K_P > \frac{r_f C_o}{V_S - V_{ref}} \frac{3}{l_S} - \frac{1}{\tau_{1x}} \left( 1 - \frac{V_{ref}}{V_S - V_{ref}} \frac{1R_{1x}}{R_L} \right)^2. \quad [1x \text{ MPVD}] \]

5. Experiment of Four-Level PWM-Based MPVD:

In this section, a closed-loop voltage-mode two-stage MPVD with four-level PWM control is designed and simulated by OrCAD tool (PSPICE). And then, the hardware implementation of the closed-loop two-stage MPVD based on PWM control is realized, and this MPVD converter is experimented for the various desired outputs. All the results are illustrated to verify the efficacy of the proposed MPVD scheme.

First, according to the proposed scheme in Fig.1, the closed-loop PWM-based MPVD is designed in circuit layout and simulated by PSPICE. Its main function is to boost the output voltage up to 4 times the supply voltage \( V_S \) (3.6V) at most for supplying the standard load \( R_L \) (600Ω). In the PWM block, the cut-off frequency \( w_L \) is taken by 628rad/sec (100Hz) for high-frequency noise rejection, and the proportional gain \( K_P \) is temporarily set on the value of 12 via (40) (Here, setting time \( \tilde{t}_S \) is assigned 2ms). Furthermore, all other simulation parameters are listed in Table 2. Based on this closed-loop MPVD, several cases are discussed as follows: (i) steady-state output, output ripple percentage and power efficiency, (ii) output robustness to source noises/disturbances, (iii) output regulation capability for loading variation, and (iv) ripple percentage and power efficiency for the various desired outputs, and hardware experimental results.

(i) Firstly, let’s consider about the steady-state response of MPVD. The closed-loop MPVD is designed to boost the output \( V_o \) up to 4 times the source \( V_S \) at most for supplying the load \( R_L \). Now, for the four desired \( V_{ref} \) of 14.0V/10.6V/7.1V/3.3V (assigned arbitrarily), the MPVDs are simulated and tested via the four-level PWM control, and then the results about the output voltages/currents and the output ripples are shown in Fig.7~10, respectively. In Fig.7(a)–10(a), it is obvious that the 4x, 3x, 2x, 1x MPVD converters has a stable work on DC-DC conversion for the various desired \( V_{ref} \), and the steady-state values of output voltages \( V_o \) are conclusively sure to follow the desired \( V_{ref} \) of 14.0V/10.6V/7.1V/3.3V after the setting time of about 2ms. From Fig. 7(b)–10(b), their relative output ripple percentages are measured as follows: \( rp = \Delta V_o/V_o = 0.059\% \), 0.0283\% , 0.2336\% , and 0.338\% , respectively. Besides, the values of power efficiency for these four cases are measured as: \( \eta = 95.88\% \), 97.96\% , 97.40\% , and 91.94\% . The theoretical ripple of (25) and power efficiency of (20)-(21) can be verified by the simulated results as here. In addition, there is a notable thing about power efficiency by using the four-level
control. If the four-level control (4x/3x/2x/1x MPVD) is not employed here, and we change over to use the one-level control (4x MPVD) only, then the values of power efficiency for the four different desired outputs are simulated as: \( \eta = 95.88\% , 72.11\% , 48.02\% , \text{ and } 21.07\% \). Obviously, it is found that the efficiency is getting worse just by using the one-level control, especially for the low-voltage desired output. Therefore, by using the four-level control, it is really helpful to improve power efficiency. The above results show that the four-level PWM-based MPVD converter has a pretty good output conversion and steady-state performance.

(ii) Secondly, let’s look at the output robustness to source disturbances. Since the source voltage is decreasing naturally with the running time of battery, or varying due to the bad quality battery, the output robustness against source noises/disturbances must be considered and emphasized. Here, there are two voltage disturbances to be discussed, including the exponential and sinusoidal noises. These two cases are illustrated as follows: (a). In the first case, it is assumed that source \( V_S \) starts at the DC value of 3.6V, and then to have a exponential decrease from 3.6V to 3.2V after 10ms, as shown in the upper half of Fig.11(a)–(b). For the two desired outputs \( V_{ref} \) of 11.5V and 6.0V, the output voltages are simulated and obtained as shown in the lower half of Fig.11(a)–(b). Obviously, the steady-state output voltage \( V_o \) is still firmly following the desired reference \( V_{ref} \), even though source \( V_S \) has decreased down to 3.2V. (b). In the second case, \( V_S \) is assumed to have the DC value of 3.6V and extra sinusoidal disturbance with peak-peak voltage of 0.4V, as shown in the upper half of Fig. 12(a)–(b). Then, the MPVD are simulated for the desired \( V_{ref} \) of 11.5V and 6.0V, and the output waveforms are obtained as shown in the lower half of Fig.12(a)–(b). Obviously, the steady-state \( V_o \) is sure to follow the desired \( V_{ref} \) of 11.5V and 6.0V respectively, in spite of the supply source with sinusoidal disturbance. So, these results show that the PWM-based MPVD converter has a good output robustness to source disturbance or noise.

(iii) Thirdly, the output regulation capability for loading variation is discussed here. For example, due to long-time running, perhaps the rising temperature causes short-circuit failure in the load unexpectedly. Thus, it results in a big variation in the load resistance. Here, we have two cases to consider as follows: (a). In the first case, the resistance value of \( R_L \) is assumed about 600\( \Omega \) normally. Suddenly, \( R_L \) has a variation from 600\( \Omega \) to 200\( \Omega \) at 20ms due to a short-circuit failure. After a short period, the load recovers from the failure, and the total value of \( R_L \) changes from 200\( \Omega \) back to 600\( \Omega \) at 40ms. Fig. 13 shows the transient waveforms of output voltage and current at the moment of the two big load variations (\( R_L = 600\Omega \rightarrow 200\Omega \rightarrow 600\Omega \)). From Fig. 13, it is obvious that the output voltage can be still regulated to hold on about 11.5V (\( V_{ref} = 11.5V \)) no matter when the load variation could be. (b). In this second case, the same load is added and connected in parallel with the output terminals at 20ms, and then the added load is moved away at 40ms. In other words, the total resistance of \( R_L \) is varying as: 600\( \Omega \)→ 300\( \Omega \)→ 600\( \Omega \). Fig. 14 shows the output voltage and current waveforms, and it is also found that the MPVD is still keeping output voltage on about 11.5V (\( V_{ref} = 11.5V \)) in spite of loading variation. Certainly, it is also found that this output current becomes double during the time interval to supply the heavier load (20ms ~ 40ms). Obviously, this closed-loop PWM-based MPVD converter has a pretty good regulation capability.

(iv) Next, the ripple percentage and power efficiency are discussed. Here, with consideration of the standard
load $R_L$ of 600Ω and the desired $V_{ref}$ from 1.0V to 14.0V, the output ripple and power efficiency of MPVD are simulated and arranged as shown in Fig. 15(a)−(b), respectively. From Fig. 15(a), it is obvious that all the output ripple percentages are lower than 0.8%. Based on the parameters in Table 2, the results are sure to agree with (25) derived theoretically. In addition, due to the four-level control employed here, it is found in Fig. 15(b) that the curve shape of the power efficiency can be divided into four parts: $0 \sim V_S$, $V_S \sim 2V_S$, $2V_S \sim 3V_S$, and $3V_S \sim 4V_S$. Obviously, the efficiency values for the most cases are higher than 70%, and the highest power efficiency can reach to 95% and above. These results show that the voltage-mode MPVD has pretty good performances for the wide desired references. Finally, based on the above design and analysis, the hardware implementation of the closed-loop PWM-based two-stage MPVD converter is realized and implemented as shown in the photo of Fig. 16. In the figure, there are two circuit boards including MPVD converter (upper) and PWM controller (lower). The layout sizes of the two circuits are $15cm \times 6cm$ and $15cm \times 9cm$ respectively, and the circuit wires are made by the prototype circuit-carving machine. For checking the closed-loop performances, the MPVD hardware circuit is tested practically (specification: Source 3.6V, load 600Ω). Then, the steady-state output voltage waveforms are measured for the different desired $V_{ref}$ of 10.5V/8.5V/6.0V/4.0V as shown in Fig.17(a)−(d), respectively (oscilloscope: Agilent Infinium 54830B). From these figures, it is obvious that the implemented MPVD has a stable work on DC-DC step-up conversion for the various desired references, and the steady-state values of output $V_o$ are sure to follow the desired $V_{ref}$ via PWM control. Besides, it is also observed that this circuit really has quite small output ripple percentages. In addition, the values of power efficiency for the different desired voltages are measured as: $\eta = 72.88\%$, 58.99\%, 41.57\%, and 27.52\% under the one-level control. If the four-level control is used, then the power efficiency can be improved as: $\eta = 95.26\%$, 78.68\%, 83.12\%, and 55.04\%. This practical converter is experimented for the various desired outputs, and the experimental results are really illustrated to verify the efficacy of the proposed scheme.

6. Conclusions

A closed-loop voltage-mode two-stage MPVD scheme is proposed by combining the four-level PWM control for the low-power DC-DC step-up/down conversion and high-efficiency regulation. In this paper, the theoretical analysis and control design are discussed, including the four-level MPVD averaging model, steady-state/transient analysis, power efficiency, conversion ratio, ripple percentage, capacitance selection, closed-loop control & stability. Finally, this closed-loop four-level PWM-based MPVD is designed by OrCAD, and its hardware implementation is realized, and then all the results are illustrated to show the efficacy of the proposed scheme. The advantages of this proposed scheme are involved as follows. (i) The SC-based MPVD scheme needs no magnetic element, so I.C. fabrication will be promising for VLSI applications. (ii) This MPVD can obtain the high voltage gain by the least number of pumping capacitors, so it will save the fabrication area more. (iii) By the four-level control employed here, the conversion efficiency can be improved much better than that just by the one-level control, especially for the low-voltage desired output. (iv) For the better output regulation, the PWM technique is adopted not only to compensate the dynamic error, but also to reinforce the output robustness against loading variations or source disturbances. (v) From stability analysis,
since the MPVD dominant pole is located in the left half of s-plane, the open-loop MPVD converter is stable. Thus, the MPVD scheme has an inherent good stability.

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References


Fig. 1 Configuration of two-stage MPVD via four-level PWM control
Fig. 2 Theoretical waveforms of the 4x MPVD
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(b) Phase II

(c) Phase IV

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Fig. 14 Output regulation capability for loading variation ($R_L : 600\Omega \rightarrow 300\Omega \rightarrow 600\Omega$)
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Fig. 17(d) Steady-state output voltage when $V_{\text{ref}} = 4$V
Table 1 Multiphase operation of MOSFETs for four-level control

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<th>Phase III</th>
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Table 2 MPVD circuit parameters

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<td>PMOS FET</td>
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