Design and Analysis of Multistage Multiphase Switched-Capacitor Boost DC-AC Inverter

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Abstract—A closed-loop multistage (n-stage) multiphase (p-phase) switched-capacitor boost DC-AC inverter (MPSCI) is proposed by combining a variable-phase control (VPC) and sinusoidal pulse-width-modulation (SPWM) technique for low-power step-up inversion/regulation. Its power stage contains two parts: MPSC booster (front) and H-bridge (rear). (i) An n-stage p-phase MPSC is for an inductor-less boost DC-DC conversion, where n voltage doublers are in series for boosting voltage gain up to 2^n at most. For improving efficiency, VPC is suggested to realize a variable multiphase operation by changing phase number p and topological path for more suitable gain level. (ii) An H-bridge is employed for DC-AC conversion, where 4 switches are controlled by SPWM not only for full-wave operation, but also for enhancing output regulation as well as robustness to source/loading variation. The analysis and design include: MPSCI model, steady-state/dynamic analysis, conversion ratio, power efficiency, stability, capacitance selection, total harmonic distortion (THD), filter and control design. Finally, the closed-loop MPSCI is simulated, and the hardware is implemented and tested. All the results are illustrated to show the efficacy of the proposed scheme.

Index Terms—multistage, multiphase, switched-capacitor (SC), boost inverter, variable-phase control, sinusoidal PWM.

I. INTRODUCTION

The SC-based power converter, possessed of charge pump, is a good solution to low-power DC-DC conversion because it has only semiconductor switches/capacitors. Unlike traditional one, a SC converter needs no magnetic element, so it always has light weight and small volume. A SC converter is usually designed for an output higher than supply voltage or a reversed-polarity voltage. This function fits many applications, e.g. OP-amp, flash EEPROM, WLED, fluorescent lamp, and LCD drivers. In fact, SC idea has existed over half a century. Up to now, many types have been suggested for power conversion [1], and some well-known topologies are (i) Dickson charge pump, (ii) Ioinovici SC, (iii) Ueno charge pump, and (iv) Makowski charge pump. In 1976, Dickson charge pump was proposed with a two-phase chain of diodes and pumping capacitors [2], and its dynamic analysis was discussed [3]. But, the drawbacks are the fixed gain and larger device area. In the period of 1990, Ioinovici et al. proposed a SC with two capacitor cells working complementarily [4]. Then, Chung and Ioinovici suggested a current-mode SC to improve the supply current waveform [5]. In 1997, Zhu and Ioinovici performed a comprehensive and accurate steady-state analysis of SC [6]. In 1998, Mak and Ioinovici suggested a SC inverter with high power density [7]. Following this, Chang proposed an intergrated step-up/down SC converter/inverter [8-9]. In 2009, Tan et al. proposed a low-EMI interleaved SC [10]. However, Ioinovici SC has the gain proportional to the number of pumping capacitors. In 1991, Ueno et al. proposed an 4-stage SC transformer idea for step-up ratio of Fibonacci series to realize an emergency power supply [11], and as well as a low ripple-noise SC [12]. However, these converters were suffering from a limited line regulation capability. In 1997, Makowski suggested a canonical structure of multiplier charge pump with two-phase cascaded voltage doublers [13]. An n-stage Makowski charge pump has the voltage gain limited by the (n+1)-th Fibonacci number [14-15]. In 2001, Starzyk proposed a multiphase voltage doubler by multiphase operation different from two-phase before [16]. The performance limits were discussed, and the relationship (phase number/voltage gain) was presented by generalized Fibonacci number [17-18]. An n-stage Starzyk charge pump can boost voltage gain up to 2^n at most, i.e. the number of pumping capacitors in Starzyk is required fewer than that in Makowski for the same gain. Nevertheless, the SC development for DC-AC is still not enough. Here, MPSC booster is presented based on Starzyk’s idea as the front stage. But, some improved spaces still exist. (i) Since Starzyk multiphase operation is fixed, the gain is also fixed. When a desired output is lower, it results in the bad efficiency. For better efficiency, VPC is suggested to realize a “variable” multiphase operation for more suitable gain level. (ii) Since Starzyk circuit scheme is fixed, the regulation capability is limited. SPWM is employed here to enhance output regulation and robustness to source/loading variation.

II. CONFIGURATION OF MPSCI

Fig. 1 shows the closed-loop MPSCI, and it contains two: “power and control unit”. The power unit: MPSC-based inverter is composed of MPSC booster and H-bridge for boost DC-AC conversion. The control unit: SPWM controller is
composed of SWPM block and variable-phase generator in charge of duty-cycle and variable-phase control (VPC).

Firstly, the MPSC booster is discussed. In Fig. 1, the n-stage p-phase MPSC booster is composed of n voltage doublers in series between source V_s and buffer capacitor voltage V_{CB}. The goal is to boost V_{CB} up to 2^n V_s at most. To simplify explanation, the stage number n is assumed 3, and the phase number p is selected no more than 2^3 = 8 (p = 1, 2, 3, ..., 8) [17]. Here, p = temporarily 8, i.e. the gain level will be 8 (8x).

For more details, it includes 3 pumping capacitors C_1, C_2, C_3, buffer capacitor C_b, and 12 MOSFETs S_1, S_2, S_3, ..., S_{12}, where each capacitor has the same value C (C_1 = C_2 = C_3 = C) with equivalent series resistance (ESR) r_c, and S_1, S_2, S_3, ..., S_{12} are operated as switches with on-state resistance r_f. Fig. 2 shows the theoretical waveforms of 3-stage 8x MPSC, where T_S is MPSC cycle (T_S = 1/f_S, f_S: MPSC frequency). Due to p = 8, one T_S has 8 phases (Phase I,II,III,...,VIII), and each phase has the same phase cycle T (T = T_S/8). Now, the Phase I-VIII operations are discussed. (i) Phase I: S_1, S_2 turn on. The topology is shown in Fig. 3(a): v_{C_1} (voltage across C_1) is charged by V_s, and C_b is discharged to supply load R_f of H-bridge. (ii) Phase II: S_3, S_4, S_5, S_6 turn on. The topology is in Fig. 3(b): V_{C_2} is charged by V_s, v_{C_1} in series, and C_b is discharged to supply R_f. (iii) Phase III: it repeats Phase I operation. (iv) Phase IV: S_7, S_8, S_9, S_10 turn on. The topology is in Fig. 3(c): V_{C_3} is charged by V_s, v_{C_1}, v_{C_2} in series, and C_b is still discharged to supply R_f. (v)-(vii) Phase V-VII: the Phase V/VI/VII operations repeat the Phase I/II/III ones. (viii) Phase VIII: S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8, S_9, S_{10}, S_{11}, S_{12} turn on. The topology is in Fig. 3(d): C_b is charged by V_s, v_{C_1}, v_{C_2}, v_{C_3} in series, and discharged to supply R_f at the same time. Since v_{C_1}/v_{C_2}/v_{C_3} is toward the goal of V_s/2V_s/4V_s, v_{CB} can be boosted to 8V_s at most. Thus, it stands to reason that the n-stage MPSC has voltage gain of 2^n at most. Table 1 shows other multiphase operations for the different p (1x, 2x, ..., 7x), where S_1 - S_{12} operations are all listed.

Secondly, the H-bridge is discussed. In Fig. 1, the H-bridge is a full-wave bridge structure between v_{CB} and v_o. The function is to convert v_{CB} (DC) into v_o (AC). For more details, it has 4 MOSFETs S_A^+, S_A^-, S_B^+, S_B^- and 4 diodes in parallel. By SPWM controller, the driver signals of S_A^+, S_A^-, S_B^+, S_B^- are generated to keep v_o on following the sinusoidal reference v_{ref}. Besides, there is a power-usage band-stop filter (BSF), including filter inductor L_F/capacitor C_F. The function is like a trap to eliminate some harmonics of v_o for better THD.

Thirdly, the SPWM controller is discussed. The controller is composed of low-pass filter (LPF), SPWM block and variable-phase generator. From signal flow, v_o is sent into LPF for high-frequency noise rejection. Then, the filtered v_o is compared with v_{ref} to obtain the tracking error e, as well as the control signal v_{con} via SPWM block. The driver signal generation of S_A^+, S_A^-, S_B^- and S_B^- is explained as follows. (i) S_A^+ is
obtained by comparing \( \nu_{\text{con}} \) with \( V_{\text{ramp}} \) (saw-toothed ramp), and its duty cycle is denoted by \( D_A \). \( S_A^+ \) is obtained by inverting \( S_A^- \), and its duty cycle is \( 1 - D_A \) (\( S_A^+ \), \( S_A^- \) are complementary). (ii) \( S_B^+ \) is obtained by comparing \( -\nu_{\text{con}} \) with \( V_{\text{ramp}} \), and its duty cycle is \( 1 - D_B \). \( S_B^- \) is obtained by inverting \( S_B^+ \), and its duty cycle is \( 1 - D_B \) (\( S_B^- \), \( S_B^+ \) are complementary), where \( -\nu_{\text{con}} \) is the opposite signal of \( \nu_{\text{con}} \).

Since \( \nu_{\text{con}} \) and \( -\nu_{\text{con}} \) are opposite, the relationship \( (D_A, D_B) \) is \( D_A + D_B = 1 \). When \( 0.5 < D_A < 1 \) (i.e., \( 0 < D_B < 0.5 \)), it presents that the ON-time interval of \( S_A^+ \), \( S_B^- \) is longer than that of \( S_A^- \), \( S_B^+ \), and then it leads to positive output of \( \nu_o \). When \( 0 < D_A < 0.5 \) (i.e., \( 0.5 < D_B < 1 \)), it presents that the ON-time interval of \( S_A^- \), \( S_B^+ \) is longer than that of \( S_A^+ \), \( S_B^- \), and so it leads to negative output of \( \nu_o \). When \( D_A = D_B = 0.5 \), it leads to zero output of \( \nu_o \). For the good of explanation, the waveform of \( S_A^+ (S_B^-) \) is defined by AND-logic combination of \( S_A^- (S_B^+) \), as shown in Fig. 4(a), and its duty cycle is denoted by \( D_A^+ (D_B^-) \) as

\[
D_A^+ = \begin{cases} 
2D_A - 1, & 0.5 \leq D_A \leq 1 \\
0, & 0 \leq D_A \leq 0.5
\end{cases} \quad D_B^- = \begin{cases} 
2D_B - 1, & 0.5 \leq D_B \leq 1 \\
0, & 0 \leq D_B \leq 0.5
\end{cases}
\]

(1)
to handle the effective positive (negative) output. Here, a more detailed explanation of (1) is given. For example, assume that \( V_{\text{ramp}} \) is a ramp from \(-1\) to \(+1\), and \( +\nu_{\text{con}} = 0.08 \) now (i.e. \( -\nu_{\text{con}} = -0.8 \)) as shown in Fig. 4(b). By comparing \( +\nu_{\text{con}} \) with \( V_{\text{ramp}} \), the waveform of \( S_A^+ \) is obtained, and its duty cycle is \( D_A = 0.9 \). Similarly, \( S_B^- \) is obtained by comparing \(-\nu_{\text{con}} \) with \( V_{\text{ramp}} \), and its duty cycle is \( D_B = 0.1 \). In addition, the waveform of \( S_A^- (S_B^+) \) is obtained by inverting \( S_A^+ (S_B^-) \). Next, by logic-AND of \( S_A^- (S_B^+) \), the waveform of \( S_A^- (S_B^+ \) is obtained, and its duty cycle is easily found as \( D_A^- = 2 \times 0.9 - 1 = 0.8 \). Also, \( S_B^- \) is obtained by logic-AND of \( S_A^- (S_B^+ \), and its duty cycle is \( D_B^- = 0 \). To conclude, \( D_A, D_B \) are the practical duty cycles in SPWM block, and \( D_A^+, D_B^- \) are the duty-cycle variables for theoretical analysis. The positive (negative) half-cycle output is regulated relative to how long \( D_A^+ T_{\text{PWM}} \) (\( D_B^- T_{\text{PWM}} \) is), where \( T_{\text{PWM}} = 1/f_{\text{PWM}} \), \( f_{\text{PWM}} \) : SPWM frequency. The MPSC frequency \( f_S \) is generally taken at 10 times or higher value of \( f_{\text{PWM}} \) for better boost performance.

Besides, VPC is proposed to realize a “variable” multiphase operation for improving efficiency, especially for lower \( \nu_{\text{ref}} \). The idea is to obtain the more suitable gain level for fitting \( pV_S \) to \( V_m \) by changing phase number \( p \) and topological path, where \( V_m \) is the AC peak of \( V_{\text{ref}} \). With programmable chip or frequency divider, a variable-phase generator is designed for VPC to do two things: (i) The generator has to determine a suitable phase number \( p = [V_m/V_S]_{\text{Gauss}} \) (\( p = 1, 2, 3 \),..., or \( 8 \)). (ii) Based on this \( p \), the generator has to generate the signals \( S_1 - S_{12} \) as shown in Table 1 so as to change topological path for this suitable gain level (1x, 2x, 3x, ..., or 8x).

A remark is given about phase number. The sufficient phase number is \( p = 4 \) for the 8x gain [18]. In our paper, the phase number is taken by \( p = 8 \) for the 8x gain. It seems to be a little redundant in execution. We have some reasons to keep the redundancy: (i) The timing-control circuit is made easier. As shown in Fig. 2, we need 3 sets of symmetrical driver signals as: \( \overline{S_1}, S_2 \) \& \( \overline{S_3}, S_4 \), \( \overline{S_5}, S_6 \) \& \( \overline{S_7}, S_8 \), \( \overline{S_9}, S_{10} \) \& \( \overline{S_{11}}, S_{12} \). It is noticeable that these waveforms are symmetrical. In one \( T_3 \) (360°), \( \overline{S_1}, S_2 \) is leading 45° ahead of \( \overline{S_3}, S_4 \), \( \overline{S_5}, S_6 \) is leading 90° ahead of \( \overline{S_7}, S_8 \), and \( \overline{S_9}, S_{10} \) is leading 180° ahead of \( \overline{S_{11}}, S_{12} \). Such a symmetrical regularity makes the realization of phase generator much easier. (ii) For \( p = 4 \), \( V_{c1} \) is charged once (Phase I) per 4 phases. In our paper, for \( p = 8 \), \( V_{c1} \) is charged 4 times (Phase I, III, V, VII) per 8 phases. Obviously, charging 4

<table>
<thead>
<tr>
<th>Table 1</th>
<th>Three-phase operations of 3-stage 1x8x MPSC booster</th>
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<tbody>
<tr>
<td>3x MPSC</td>
<td>( S_1 ), ( S_2 )</td>
</tr>
<tr>
<td>2x MPSC</td>
<td>( S_1 ), ( S_2 )</td>
</tr>
<tr>
<td>1x MPSC</td>
<td>( S_1 ), ( S_2 )</td>
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times per 8 phases is more helpful to boosting response, even though the total cycle of \( p = 8 \) is 1/2 cycle longer than that of \( p = 4 \). Of course, we need a larger buffer capacitor \( C_b \), but not very large. If \( p = 4 \), \( C_b \) has to stand up alone for 3/4 cycle to supply the load. In our paper (\( p = 8 \)), \( C_b \) has to supply the load alone for 7/8 cycle. By comparing the two cases, our \( C_b \) is needed just 7/6 times the value of \( C_b \) of \( p = 4 \).

### III. Formulation of MPSCI

#### A. Formulation of MPSCI booster:

First, the Thevenin model of 3-stage 8x MPSCI is derived. Now, we remove H-bridge from the power unit, and set the circuit open temporarily. Based on Fig. 3(a)-(d), the state equations for Phase I–VIII can be derived as follows.

**Phase I,II,VII:** (Fig. 3(a))

\[
\begin{align*}
&\begin{bmatrix}
v_{c1}'(t) \\
v_{c2}'(t) \\
v_{c3}'(t) \\
v_{c4}'(t)
\end{bmatrix} =
\begin{bmatrix}
-1 & 0 & 0 & 0 \\
0 & -1 & 0 & 0 \\
0 & 0 & -1 & 0 \\
0 & 0 & 0 & -1
\end{bmatrix}
\begin{bmatrix}
v_{c1}(t) \\
v_{c2}(t) \\
v_{c3}(t) \\
v_{c4}(t)
\end{bmatrix} +
\begin{bmatrix}
1 & 0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
I \\
V_S
\end{bmatrix}.
\end{align*}
\]

**Phase II,VI:** (Fig. 3(b))

\[
\begin{align*}
&\begin{bmatrix}
v_{c1}'(t) \\
v_{c2}'(t) \\
v_{c3}'(t) \\
v_{c4}'(t)
\end{bmatrix} =
\begin{bmatrix}
-1 & 0 & 0 & 0 \\
0 & -1 & 0 & 0 \\
0 & 0 & -1 & 0 \\
0 & 0 & 0 & -1
\end{bmatrix}
\begin{bmatrix}
v_{c1}(t) \\
v_{c2}(t) \\
v_{c3}(t) \\
v_{c4}(t)
\end{bmatrix} +
\begin{bmatrix}
1 & 0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
I \\
V_S
\end{bmatrix}.
\end{align*}
\]

**Phase IV:** (Fig. 3(c))

\[
\begin{align*}
&\begin{bmatrix}
v_{c1}'(t) \\
v_{c2}'(t) \\
v_{c3}'(t) \\
v_{c4}'(t)
\end{bmatrix} =
\begin{bmatrix}
-1 & 0 & 0 & 0 \\
0 & -1 & 0 & 0 \\
0 & 0 & -1 & 0 \\
0 & 0 & 0 & -1
\end{bmatrix}
\begin{bmatrix}
v_{c1}(t) \\
v_{c2}(t) \\
v_{c3}(t) \\
v_{c4}(t)
\end{bmatrix} +
\begin{bmatrix}
1 & 0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
I \\
V_S
\end{bmatrix}.
\end{align*}
\]

**Phase VIII:** (Fig. 3(d))

\[
\begin{align*}
&\begin{bmatrix}
v_{c1}'(t) \\
v_{c2}'(t) \\
v_{c3}'(t) \\
v_{c4}'(t)
\end{bmatrix} =
\begin{bmatrix}
-1 & 0 & 0 & 0 \\
0 & -1 & 0 & 0 \\
0 & 0 & -1 & 0 \\
0 & 0 & 0 & -1
\end{bmatrix}
\begin{bmatrix}
v_{c1}(t) \\
v_{c2}(t) \\
v_{c3}(t) \\
v_{c4}(t)
\end{bmatrix} +
\begin{bmatrix}
1 & 0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
I \\
V_S
\end{bmatrix}.
\end{align*}
\]

where \( R_p = 2r_f + r_C \) is the parasitic resistance for charging \( C \), and \( R_b = 6r_f + r_C \) is the parasitic resistance for charging \( C_b \) in Phase VIII. In this paper, we assume that the MPSCI booster is operating in fast-switching-limit (FSL) mode only [18]. So, by state-space averaging (SSA) technique in FSL, i.e. \( [(2) + (3) + (2) + (4) + (2) + (3) + (2) + (5)] / 8 \), the state equation of 3-stage 8x MPSCI booster can be derived as

\[
x_{c8}'(t) = A_{c8} \cdot x_{c8}(t) + B_{c8} \cdot V_S, \quad v_{c8}(t) = C_{c8} \cdot x_{c8}(t),
\]

where

\[
x_{c8}(t) = \begin{bmatrix}
v_{c1}(t) \\
v_{c2}(t) \\
v_{c3}(t) \\
v_{c4}(t)
\end{bmatrix},
\]

\[
A_{c8} = \begin{bmatrix}
2 & 1 & 0 & 0 \\
1 & 0 & 1 & 0 \\
1 & 0 & 0 & 1 \\
0 & 1 & 0 & 1
\end{bmatrix}, \quad B_{c8} = \begin{bmatrix}
1/8 & 1/8 & 0 & 0 \\
1/8 & 1/8 & 0 & 0 \\
0 & 0 & 1/8 & 0 \\
0 & 0 & 0 & 1/8
\end{bmatrix}, \quad C_{c8} = \begin{bmatrix}
1/8 & 0 & 0 & 0
\end{bmatrix}.
\]

Based on (6), its first-order equivalent model will be derived. In the first-order model, there are two parameters: boosting gain and dominant pole. By substituting \( x = 0 \) of (6), the steady-state buffer capacitor voltage \( V_{c0} \) can be obtained as

\[
v_{c0} = \left( -C_{c8} A_{c8}^{-1} B_{c8} \right) V_S = 8 \cdot V_S.
\]

Clearly, the boosting gain is 8. In fact, the gain is lower than 8 when the load is added in. Next, \( A_{c8} \) is divided into 4 sub-matrices \( A_{11} \sim A_{12} \) as (7b), and decomposed as (9a), where \( \Delta_{c8} \) is obtained as (9b) when \( C_b \geq 100 \cdot C \).

\[
A_{c8} = \begin{bmatrix}
J & 0 & 0 & 0 \\
1 & 0 & 1 & 0 \\
0 & 0 & 1 & 0 \\
0 & 0 & 0 & 1
\end{bmatrix}, \quad \Delta_{c8} = \begin{bmatrix}
1 & 0 & 0 \\
1 & 0 & 1 \\
0 & 1 & 0 \\
0 & 0 & 1
\end{bmatrix}, \quad \Delta_{c8}^{-1} A_{12} = \begin{bmatrix}
1 & 0 & 0 \\
0 & 1 & 0 \\
1 & 0 & 0 \\
0 & 0 & 1
\end{bmatrix}
\]

For better DC quality, \( C_b \) must be chosen larger. Here, \( C_b \) is taken by 100 times or larger value of \( C \). Based on this, it is obvious that \( \Delta_{c8} \) of (9b) is the dominant pole of the booster. By combining (8) and (9b), the first-order model of 3-stage 8x MPSCI booster is obtained as

\[
v_{c8} = 8 \cdot (11 \cdot R_p + R_b) \cdot C_b \cdot s + 1.
\]

By the same process, the first-order model of n-stage \( p \)-phase MPSCI is also derived as

\[
v_{c8} = \frac{p \cdot V_S}{p \cdot (tot \cdot R_p + R_b) \cdot C_b \cdot s + 1},
\]

where \( tot \) represents the total number of passing through \( C \) in Phase I,II,III,\ldots,\( p \)-1 (\( p = 1, 2, 3, \ldots, or 2^n \)). Based on (11), the Thevenin model of MPSCI booster is presented in Fig. 5, where \( R_{tot} = p \cdot (tot \cdot R_p + R_b) \) is the equivalent impedance of MPSCI booster. In addition, since the scheme is in FSL mode, this impedance is frequency-independent [18].

#### B. Formulation of MPSCI-Based Inverter:

As above, the effective positive (negative) output of \( v_{c8} \) is controlled by \( D_{AB}^- \) (\( D_{AB}^+ \)). Thus, it is concluded that H-bridge contains 4 different modes as follows:

1. **Mode I** (\( v_{c8} > 0 \)): \( D_{AB}^- = 2D_{AB} - 1 \), for \( 0.5 \leq D_{AB} \leq 1 \),
2. **Mode II** (\( v_{c8} > 0 \)): \( D_{AB}^- = 0 \), for \( 0 \leq D_{AB} \leq 0.5 \),
3. **Mode III** (\( v_{c8} < 0 \)): \( D_{AB}^- = 2D_{AB} - 1 \), for \( 0.5 \leq D_{AB} \leq 1 \),
4. **Mode IV** (\( v_{c8} < 0 \)): \( D_{AB}^- = 0 \), for \( 0 \leq D_{AB} \leq 0.5 \).

In Mode I: \( S_A, S_B \) turn on within the period of \( D_{AB}^- \cdot T_{PWM} \).
Fig. 5. Thevenin equivalent model of MPSC booster

Fig. 6. MPSCI topologies for Mode (a) I, (b) II, (c) III, (d) IV.

By combining Fig. 5, the Mode I topology is obtained as Fig. 6(a), and the dynamic equation for Mode I is derived as

$$
\begin{bmatrix}
\dot{v}_{c1}(t) \\
\dot{i}_{c1}(t) \\
\dot{v}_{c2}(t)
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 \\
-1/C_f & 0 & 0 \\
-1/C_s & 0 & 0
\end{bmatrix}
\begin{bmatrix}
v_{c1}(t) \\
i_{c1}(t) \\
v_{c2}(t)
\end{bmatrix}
+ \begin{bmatrix}
0 \\
0 \\
\frac{1}{R_s C_t}
\end{bmatrix} \cdot V_S
$$

(12)

where \( i_{c1} / v_{c2} \) is the filter inductor current/capacitor voltage, and \( i_{c1} \) is the current of \( pV_S \). In Mode II: \( S_A, S_B, S_A \), or \( S_B \) turn on within \((1-D_{AB}) \cdot T_{PWM} \). The topology is in Fig. 6(b), and the dynamic equation for Mode II can be obtained as

$$
\begin{bmatrix}
\dot{v}_{c1}(t) \\
\dot{i}_{c1}(t) \\
\dot{v}_{c2}(t)
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 \\
-1/L_f & 0 & 0 \\
-1/R_s C_t & 0 & 0
\end{bmatrix}
\begin{bmatrix}
v_{c1}(t) \\
i_{c1}(t) \\
v_{c2}(t)
\end{bmatrix}
+ \begin{bmatrix}
0 \\
0 \\
\frac{1}{R_s C_t}
\end{bmatrix} \cdot V_S
$$

(13)

By using SSA, (12): \( D_{AB} \cdot T_{PWM} \), the state equation of MPSCI is \( v_{con} > 0 \) can be derived as

Similarly, based on the topologies in Fig. 6(c)/6(d), the Mode III/IV equations can be formed. And then, by using SSA, the state equation of MPSCI for \( v_{con} < 0 \) is also derived as:

$$
\begin{bmatrix}
\dot{v}_{c1}(t) \\
\dot{i}_{c1}(t) \\
\dot{v}_{c2}(t)
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 \\
-1/L_f & 0 & 0 \\
-1/D_{AB} & 0 & 0
\end{bmatrix}
\begin{bmatrix}
v_{c1}(t) \\
i_{c1}(t) \\
v_{c2}(t)
\end{bmatrix}
+ \begin{bmatrix}
0 \\
0 \\
\frac{1}{R_s C_t}
\end{bmatrix} \cdot V_S
$$

(14)

For the good of explanation, we define an integrated duty cycle \( D \) as (i) \( D = D^-_{AB}, v_{con} > 0 \); (ii) \( D = -D^-_{AB}, v_{con} < 0 \). Based on this definition, a full-wave signal \( S_{AB} \) is obtained by combining \( S^-_{AB} \) and \( S^+_{AB} \), as shown in Fig. 4(a), and its duty cycle is just \( D \) with the range: \(-1 \leq D \leq 1 \). When \( 0 \leq D \leq 1 \) (\(-1 \leq D \leq 0 \)), it means that the positive (negative) half-cycle of \( v_o \) is running. So, based on (14)-(15) and this \( D \), the state-space description of \( n \)-stage p-phase MPSCI can be derived as

$$
\begin{bmatrix}
x(t) \\
y(t)
\end{bmatrix} =
\begin{bmatrix}
A_{in} & A_{out} \\
B_{in} & B_{out}
\end{bmatrix}
\begin{bmatrix}
x(t) \\
y(t)
\end{bmatrix}
+ \begin{bmatrix}
0 \\
0
\end{bmatrix} \cdot u(t)
$$

(16a)

where

$$
x(t) = \begin{bmatrix} v_{c1}(t) & i_{c1}(t) & v_{c2}(t) \end{bmatrix}^T, y(t) = \begin{bmatrix} v_o(t) & i_{c1}(t) \end{bmatrix}^T
$$

(17a,b,c)

$$
A_{in} = \begin{bmatrix}
0 & 0 \\
0 & 0
\end{bmatrix}
, B_{in} = \begin{bmatrix}
0 \\
0
\end{bmatrix}
$$

(17d,e)

$$
C_{in} = \begin{bmatrix}
0 & 0 \\
0 & 0
\end{bmatrix}
$$

(17f)

IV. ANALYSIS AND DESIGN OF MPSCI

A. Steady-State and Dynamic Analysis:

First, all variables of (16) are treated as: \( v_{c1}(t) = v_{c1}(t), v_{c2}(t) = v_{c2}(t), i_{c1}(t) = i_{c1}(t), i_{c2}(t) = i_{c2}(t), v_{c3}(t) = v_{c3}(t), D(t) = D(t), v_o(t) = v_o(t), \) and \( i_o(t) = i_o(t) \), where \( v_{c1}, i_{c2}, v_{c3}, D, v_o, i_o \) are the static signals, and \( v_{c1}, v_{c2}, i_{c1}, s_1, s_2, d, v_o, i_o \) are the dynamic small signals. By substituting \( x = 0 \) of (16), the steady-state output voltage \( V_o \), output current \( I_o \), and supply-terminal current \( I_S \) can be derived as

$$
I_S = -C_{inv2} \cdot A_{inv}^{-1} \cdot B_{inv} \cdot u = \begin{bmatrix} D & 0 \\
0 & 0
\end{bmatrix} \cdot \begin{bmatrix} v_o \\
I_o
\end{bmatrix}
$$

(18c)
where $C_{inv1}/C_{inv2}$ are the 1st/2nd row of $C_{inv}$. Based on (18a), $V_w$ is regulated by $D$, and even the polarity of $V_w$ is also changed because $-1 \leq D \leq 1$. Besides, $I_S = |I_S|$ is reasonable because $I_S$ has no negative current at $pV_S$ (MPSC booster). Next, based on (16), by small-signal analysis (on a duty cycle $D$), the dynamic transfer function can be derived as

$$
G(s) = \frac{V_o(s)}{V_i(s)} = \frac{\frac{2}{D} \frac{pV_S}{R_m C_f}}{1 + \frac{pV_S}{R_m C_f} + \frac{1}{2 D R_m C_f}} \left( \frac{C_d}{C_m} + \frac{R_d}{R_m + 2 D} \right) \left( \frac{C_o}{C_m} + \frac{R_o}{R_m + 2 D} \right),
$$

(19)

where $G(s)$ results from the power-usage output filter of BSF, and $G_C(s)$ comes from the booster and loading effect, and its maximum is really close to $pV_S$ when $R_L \gg r_T, r_C$.

B. Conversion Ratio and Power Efficiency:

Based on (18a), the conversion ratio $M_{inv}$ is suggested as

$$
M_{inv} = \frac{V_o}{V_i} = \frac{p D}{1 + (2 D + \frac{1}{R_m C_f}) |D| / |R_L|}. \tag{20}
$$

If $D = 0$, then $M_{inv} = 0$. If $D = \pm 1$ ($D = -1$), then the maximum (minimum) of $M_{inv}$ is close to $p$ ($-p$) when $R_L \gg r_T, r_C$, i.e. $V_o$ is converted to $-pV_S - pV_S$. Normally, the maximum attainable output $V_o$ is $pV_S$ – voltage drops in the charging and discharging circuits. Thus, $R_L$ is asked much larger than $r_T, r_C$. In fact, $R_L$ is $\Omega$-level, and $r_T, r_C$ is in m2-level.

Next, the power efficiency is discussed. Here, the duty cycle is assumed as $D = D_m - \sin(\omega t)$, $0 \leq D_m \leq 1$, i.e. $V_o$ is desired sinusoidal ($V_o = V_m - \sin(\omega t)$), $0 \leq V_m \leq pV_S$, where $\omega_o = 2 \pi f_o$ is the output frequency. Thus, the input power $P_i$ and output power $P_o$ can be obtained as

$$
P_i = pV_S I_S = \frac{2 p V_m \pi}{\sqrt{2}} \int_0^{2 \pi} \sin(\omega t) d\omega t = \frac{2}{\pi} pV_m V_i, \tag{21a}
$$

$$
P_o = V_o \sin^{-1} (V_o) = \int_0^{2 \pi} V_o d\omega t = \frac{V_m}{\pi} \int_0^{2 \pi} V_o d\omega t.
$$

(21b)

Thus, the efficiency $\eta_{inv}$ of MPSCI can be derived as

$$
\eta_{inv} = \frac{P_i}{P_o} = \frac{\pi}{4} \frac{V_m}{V_o} \frac{\pi}{1 + (2 \pi D_m + \frac{R_o}{R_m})} / R_L. \tag{22}
$$

If $r_T, r_C$ are small enough to be neglected, then the maximum of $\eta_{inv}$ is 78.5%. $\eta_{inv}$ is higher when the AC peak $V_m$ is closer to $pV_S$. But, if $V_m$ is much lower than $pV_S$, then $\eta_{inv}$ is quite bad. Here, for better efficiency, VPC is used to change phase number $p$ for fitting $pV_S$ to $V_m$ as close as possible. For example, $V_m$ is 3.6V, and $V_m$ is adjusted at 17.5V. If $p = 8$, the best efficiency is 47.7%. If $p = 7$, the best value is 54.5%. If $p = 6$, the best is 63.6%. But, if $p = 5$, the best efficiency is improved to 76.4%. The reason is that $V_{inv}$ is the closest to $V_m$ at 17.5V. Finally, a remark is given about comparison to Zhu [6]. Zhu’s circuit is an n-stage 2-phase SC, so the maximum gain is proportional to $n$. Since $n$ is fixed, it results in the bad efficiency when the lower output is desired. Exactly, some of our results are similar to [6], but we have two differences: (i) Our booster is an n-stage p-phase SC, so the maximum gain is $2^p$. (ii) Since $p$ is “variable” by VPC, the efficiency is improved, especially for lower output voltage.

C. Stability and Capacitance Selection:

Based on (17d), the characteristic equation is derived as

$$
\Delta_0 = \delta - A_m = \left[1 + \frac{1}{C_s (R_m + 2 D) / L_p} \right] \left[1 + \frac{2 D \frac{R_d}{R_m + 2 D} / L_p} {1 + \frac{1}{C_o (R_m + 2 D)}} \right] > 0, \tag{23}
$$

where the 1st 2nd fractional term is relative to MPSCI booster (H-bridge). Thus, the characteristic roots can be obtained as

$$
p_1 = \frac{1}{C_s (R_m + 2 D)} \left[1 + \frac{1}{C_o (R_m + 2 D)} \right], \tag{24a}
$$

$$
p_2 = \frac{2 D \frac{R_d}{R_m + 2 D} / L_p} {1 + \frac{1}{C_o (R_m + 2 D)}} > 0, \tag{24b}
$$

Based on (24a), MPSCI booster is stable because $p_1$ is in the left half of s-plane. Based on (24b), the H-bridge is stable because $p_2$ has the negative real part when $L_p / C_p \geq \omega^2$. So, the open-loop MPSCI has an inherent good stability.

Next, the selection of $C, C_o$ is discussed. Based on Fig. 3(a), the phase time constant $R_o C$ must be smaller than phase cycle $T = T_{S} / 8$ for faster boosting. In addition, in Fig. 3(a)-(c), $C_o$ stands alone to supply $R_L$ (Phase I-VII), so the discharging time constant $R_o C_o > T_S$ is asked. Let’s extend these for n-stage p-phase, and then the time inequality is obtained as:

$$
R_o C < T_S / p < T_S < R_L C_o. \tag{25}
$$

Based on (25), $C_o$ should be chosen larger for DC quality of $V_{ch}$, and $C$ should be smaller for boosting response. So, (25) provides for the capacitance selection of $C, C_o$. Here, the MPSCI phase cycle $T$ is really much shorter than the time constant $R_o C_o$ at output, so the SSA analysis can be valid.

D. THD and Filter Design:

Based on Fig. 4(a), the detailed waveform of $S_{AB}$ is plotted in Fig. 7 ($T_o = 1 / f_o = 2 \pi f_o \omega_o$). Now, assume that the output filter has not been added in, $v_o(t)$ can be formed as

$$
v_o(t) = \sum_{n=-1}^{N} V_m \sin((n + 1) \omega_o t) + P_e(t), \tag{26}
$$

where $q = T_o / T_{PWM}$ ($q = f_{PWM} / f_o$), and a pulse function is defined by $P_e(t) = u(t - t_{+1}) - u(t - t_{-2})$ between $t_{+1}$ and $t_{+2}$ ($t_{+1} = k + (1 - D_{ij}) / 2 T_{PWM}$, $t_{+2} = k + (1 + D_{ij}) / 2 T_{PWM}$) with the duty cycle $D_i = D_m \cdot \sin(2 \pi / q k)$, $k = 0.1, 2, ..., q - 1$. Because $v_o(t)$ is odd, the Fourier series of $v_o(t)$ is expressed as (27a), where $A_n$ is shown in (27b) ($\theta_{+1} = \omega_o - t_{+1}$, $\theta_{+2} = \omega_o - t_{+2}$).

$$
v_o(t) = \sum_{n=1}^{N} A_n \sin(n \omega_o t), \tag{27a}
$$

$$
A_n = \frac{2}{T_o \int_{-T_o/2}^{T_o/2} v_o(t) \sin(n \omega_o t) d t} = \frac{2 V_m}{\pi n} \sum_{k=0}^{q-1} \sin(n \omega_o t_{+1}) - \cos(n \omega_o t_{+2}) \tag{27b}
$$

Based on (27b), $A_n$ is obtained as shown in Fig. 8, and THD is $\sqrt{A_1^2 + A_2^2 + \cdots + A_{2n}} / A_1 = 46.85\%$. Clearly, the harmonics always occur at $n = q, 2q, 3q, ...$ (i.e. $f_o / q, 2f_o / q, 3f_o / q, ...$). Now, let’s add the BSF: $G_{s}(s)$ of (19). Based on (19), the center frequency $o_f$ and quality factor $Q$ can be obtained as
 PWM block, $s/f_o \geq 18$ results in higher THD. Based on (28b), $L_P/C_P \geq r_f$ is equivalent to $Q \geq 0.5$. So, $L_P$ and $C_P$ can be designed as:

$$L_P \geq \frac{r_f}{2\pi \cdot q \cdot f_o}, \quad C_P \leq \frac{1}{2\pi \cdot q \cdot f_o \cdot r_f}.$$  

(29a,b)

For smooth frequency response, $Q$ should not be too big. $Q$ is generally smaller than 1. Thus, $L_P$ is suggested not to exceed twice the value of $Q$. By the same process, other output filters can be also designed to trap higher harmonics. By using the $q_{f_o}$ design, THD is improved to 24.64%. If adding the $2q_{f_o}$ design, THD is reduced to 13.60%. Also, it is practicable that we add a small bypass capacitor $C_{bypass}$ at the output terminal to bypass the high-order harmonics ($2q_{f_o}, 3q_{f_o}, ...$).

**E. Control Design:**

In the LPF, there is a cut-off frequency $o_c$ chosen according to what range the possible noises occur at. Certainly, to avoid affecting MPSCI response, $o_c$ is generally taken higher than output frequency $o_{L}$ ( $o_c > o_{L}$). Next, via the SPWM block, the main job is to keep $V_o$ on top of following $V_{ref}$. Fig. 8 shows the control diagram, where a gain $K_p$ is to compensate error, rise or settling time. If $V_o$ or $R_L$ is decreasing, then $V_o$ will be going down. The error $e$ between $V_{ref}$ and $V_o$ is rising quickly. The bigger $e$ makes a larger duty cycle $D$ via $K_p$, and then the larger $D$ (line/load regularity) can be enhanced.

Now, the $K_p$ design is discussed. Assume that the MPSCI is running around a duty cycle $D$ for some desired $V_{ref}$. In other words, $V_o$ is equal to $V_{ref}$ under this $D$. Based on Fig. 8 and (19), the closed-loop characteristic equation of $n$-stage PWM MPSCI can be derived as:

$$\Delta_n(s) = 1 + H(s) = 1 + \left[ K_p \cdot \frac{pV_{ref} \cdot R_L}{R_L + 2r_f} \cdot \frac{1}{r_f C_P} \right] = 0.$$  

(30)

When we consider the dynamic response at the frequency lower than $o_c$ in LPF, (30) can be approximated to

$$\Delta_n(s) = 1 + H(s) = 1 + \left[ K_p \cdot \frac{pV_{ref} \cdot R_L}{R_L + 2r_f} \cdot \frac{1}{r_f C_P} \right] = 0.$$  

(31)

So, the settling time $t_s$ within a settling error of ±5% can be

$$t_s = 3 \cdot R_{bus} C_b \left[ \frac{1 + K_p \cdot \frac{pV_{ref} \cdot R_L}{R_L + 2r_f}}{r_f C_P} \right].$$  

(32)

For keeping $t_s$ shorter than the desired settling time $t_{ref}$, the gain of $K_p$ can be designed as

$$K_p = \frac{R_L + 2r_f}{pV_{ref} \cdot R_L} \left[ \frac{1}{R_{bus} C_b} \cdot \frac{3 \cdot R_{bus} C_b}{t_{ref}} - 1 \right].$$  

(33)

Next, let the phase margin be higher than some desired $\theta_d$. As $PM = 180^\circ - \angle H(j\omega_0) > \theta_d$ where $\omega_0$ is the gain crossover frequency of $H(s)$, the phase margin is designed for boosting $K_p$ to have a higher and desired $\theta_d$. So, $\omega_0$ is obtained as:

$$\omega_0 = \frac{1}{R_{bus} C_b} \left[ \frac{K_p \cdot pV_{ref} \cdot R_L}{R_L + 2r_f} \right] - 1.$$  

(34)

By substituting (34) into the inequality of $PM$, the maximum gain of $K_p$ for the desired $\theta_d$ can be derived as:

$$K_p = \frac{R_L + 2r_f}{pV_{ref} \cdot R_L} \cdot sec(\theta_d).$$  

(35)

V. EXAMPLE OF MPSCI

First, the closed-loop MPSCI ($n = 3$) is designed by PSPICE for simulation, where the MPSCI booster is realized for boosting $V_C$ up to $8 \cdot V_S$ at most ($V_S = 3.6V$), and the H-bridge is for DC-AC conversion to supply load $R_L$ ($R_L = 4k\Omega$). The parameters are listed: $f_s = 100kHz$, $f_{SPWM} = 40kHz$, $C = 10\mu F$, $C_b = 1m\mu F$, $r_f = 20m\Omega$, $\tau_C = 180\mu s$. In the controller, $o_{L}$ is taken by $6kHz$ for high-frequency noise rejection. By (34), $K_p$ is designed at 0.08 for $t_S = 15ms$ and $\theta_d = 45^\circ$. Based on (29) and $f_o = 1kHz$ ( $q = 40$), the filter inductor/capacitor are chosen as: $L_F = 150nH$, $C_F = 1066\mu F$. Besides, for better THD, a small bypass capacitor $C_{bypass} = 5nF$ is used here. Now, the simulation cases are discussed as: (i) steady-state response, and (ii) source/loading variation. In the end, the MPSCI hardware is implemented, and tested for the same cases.

(i) The steady-state response is discussed. The closed-loop $8x/6x/4x$ MPSCI is simulated for AC peak $V_m = 28V/21V/14V$ (assigned arbitrarily), and the waveforms of $V_o$ are shown in Fig. 10. Clearly, the MPSCI is stable for DC-AC conversion, i.e. $V_o$ are really following $V_{ref}$, and the settling time is shorter than $t_{ref} = 15ms$. The VPC-based efficiencies and THDs for $V_m = 28V/21V/14V$ are obtained as: $\eta = 76.6\%$, $76.2\%$, $75.8\%$, $THD = 3.36\%$, $3.22\%$, $3.29\%$. If we just use the “fixed” $p = 8$ (without VPC), the efficiencies are obtained:
Fig. 10. Output $v_o$ for the different $V_{ref}$: $f_o = 1 \text{kHz}$ and AC peaks $V_m = (a) 28 \text{V}$, (b) 21 \text{V}, (c) 14 \text{V}$.

Fig. 11. Power efficiencies for the various (a) references, (b) loading.

$\eta = 76.0\%$, 56.9\%, 37.7\%. Clearly, $\eta$ without VPC become worse when the desired output is lower. Fig. 11(a) shows the efficiency curves for $V_m = 1.2 \text{V} \sim 28.0 \text{V}$ ( $R_L = 4 \Omega$), where the bold line is $\eta$ with VPC, and the dotted line is $\eta$ without VPC. The bold curve has 8 divisions, and the results correspond to (22). By comparing the curves, it is obvious that $\eta$ with VPC is much better than $\eta$ without VPC, especially for the lower output voltage. Fig. 11(b) shows the efficiency curves for $R_L = 0.5 \text{k}\Omega \sim 7.5 \text{k}\Omega$ ( $V_m = 28 \text{V}$), where the bold line is $\eta$

with $r_T = 20 \text{m}\Omega$, $r_C = 18 \text{m}\Omega$, and the dotted line is $\eta$ with $r_T = 0.4 \Omega$, $r_C = 0.36 \Omega$. By comparing the curves, it is obvious that $\eta$ with smaller parasitic is much better than $\eta$ with bigger parasitic, especially for the heavier loading.

(ii) The source/load variation are discussed. Here, we have 3 cases as follows. ($V_m = 27 \text{V}$, $f_o = 1 \text{kHz}$) (A): Exponential disturbance: $V_S$ is 3.6V plus an exponential drop from 3.6V to 3.4V, as shown in the upper of Fig. 12(a). Then, $v_o$ is shown in the lower of Fig. 12(a). Clearly, $v_o$ is following $V_{ref}$, even though $V_S$ has decreased to 3.4V. (B): Sinusoidal disturbance: $V_S$ is 3.6V plus sinusoidal disturbance of 0.4V$_{p-p}$, as shown in the upper of Fig. 12(b). Then, $v_o$ is shown in the lower of Fig. 12(b). Clearly, $v_o$ is still following $V_{ref}$ in spite of source disturbance. (C): Load failure: $R_L$ is 4k\Omega normally, and it changes from 4k\Omega to 0.5k\Omega at 40ms due to failure. After a short period, it is from 0.5k\Omega to 4k\Omega at 70ms. Fig. 12(c) shows $v_o$ when $R_L = 4 \Omega \rightarrow 0.5 \Omega \rightarrow 4 \Omega$. As error $e$ is bigger during the failure, $v_o$ is still following $V_{ref}$.

Finally, the hardware of closed-loop MPSCI is implemented as shown in the photos of Fig. 13. There are 3 circuit boards including: 3-stage MPSC booster and variable-phase generator (14cm by 9cm), H-bridge (8cm by 12cm), and SPWM (8cm by 12cm). Next, this hardware circuit is tested practically for the cases of steady-state response and source/loading variation ( $V_m = 3.0 \text{V}$, $R_L = 6.8 \text{k}\Omega$, Agilent Infiniium 54830B oscilloscope: signal attenuation rate: 4.7 times). (i) The steady-state response is discussed. Fig. 14 shows $v_o$ for the various $V_{ref}$ ( $V_m = 22 \text{V}$ /
16V/10V, \( f_0 = 1kHz \). In Fig. 14(a), \( V_{o,pp} \) is 9.38V, i.e. the AC peak of \( v_o \) is 22.04V (9.38V × 4.7/2 = 22.04V), and practical \( f_0 = 1005.3Hz \). In Fig. 14(b), \( V_{o,pp} \) is 8.66V, i.e. the peak of \( v_o \) is 16.12V (6.86V × 4.7/2 = 16.12V), and practical \( f_0 = 1005.4Hz \). In Fig. 14(c), \( V_{o,pp} \) is 4.30V, i.e. the peak of \( v_o \) is 10.11V (4.30V × 4.7/2 = 10.11V), and \( f_0 = 1005.2Hz \) practically. Clearly, MPSCI is stable for DC-AC conversion, and \( v_o \) are really following \( V_{ref} \). Besides, the efficiency and THD of 8x/6x/4x MPSCI are measured as: \( \eta = 70.5\% , 66.9\% , 62.8\% \), THD = 9.7\%, 8.9\%, 8.1\%. If we just use 8x MPSCI, then \( \eta = 70.5\% , 50.2\% , 31.4\% \) (without VPC). Really, VPC is useful for improving efficiency.

(ii) The cases of source/loading variation is considered. (A): For different \( V_S = 3.0V/2.8V, v_o \) are measured as shown in Fig. 14(a)/15(a) \( V_m = 22V, f_o = 1kHz \). In Fig. 14(a), \( V_{o,pp} \) is 9.38V when \( V_S = 3.0V \), i.e. the peak of \( v_o \) is 22.04V (9.38V × 4.7/2 = 22.04V). In Fig. 15(a), \( V_{o,pp} \) is 9.32V when \( V_S = 2.8V \), i.e. the peak of \( v_o \) is 21.90V (9.32V × 4.7/2 = 21.90V). By comparing these results, it is found that \( v_o \) is still following \( V_{ref} \), even though \( V_S = 3.0V \) \( \rightarrow \) 2.8V. (B): \( V_S \) is 3.0V plus sinuosidal disturbance of 0.2V, as shown in the upper of Fig. 15(b), \( v_o \) is shown in the lower of Fig. 15(b) \( (V_m = 22V , f_o = 1kHz) \). \( V_{o,pp} \) is 9.35V, i.e. the peak of \( v_o \) is 21.97V (9.35V × 4.7/2 = 21.97V). \( v_o \) is still following \( V_{ref} \) in spite of source disturbance. (C): When the loading is added triple \( (R_L = 6.8k\Omega \rightarrow 2.2k\Omega) \), \( v_o, V_{ref} \) are measured in Fig. 15(c) \( V_m = 22V , f_o = 1kHz) \). \( V_{o,pp} \) is 9.31V, i.e. the peak of \( v_o \) is 21.88V (9.31V × 4.7/2 = 21.88V), and practical \( f_0 = 1005Hz \). So, the MPSCI still keeps \( v_o \) on following \( V_{ref} \), even though the loading is triple.

VI. CONCLUSION

A closed-loop \( n \)-stage \( p \)-phase MPSCI is proposed by using VPC and SPWM for step-up DC-AC conversion and regulation, and the relevant theoretical analysis and design are presented. Finally, the closed-loop MPSCI is simulated, and the hardware is implemented and tested. All the results are illustrated to show the efficacy of the proposed scheme. The advantages of the scheme are as follows. (i) The SC-based MPSCI needs no large magnetic element (except BSF), so I.C. fabrication is promising. (ii) The \( n \)-stage MPSCI booster has voltage gain of \( 2^n \) at most, so the number of pumping capacitors is needed less. (iii) VPC is suggested to improve efficiency because it can realize a variable multiphase operation by changing phase number \( p \) and topology for the more suitable gain level. Thus, the VPC-based efficiency is better than that just by the fixed phase operation, especially for the lower output. (iv) SPWM is adopted to enhance output regulation as well as robustness to
source/loading variation. (iv) Because the poles are in the left half of s-plane, the open-loop MPSCI is stable. So, the proposed scheme has an inherent good stability.

ACKNOWLEDGMENT

This research of converter circuit theory and application is financially supported by National Science Council of Taiwan, R.O.C., under Grant NSC 98-2221-E-324-024.

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