Modeling and Implementation of High-Gain Switched-Inductor Switched-Capacitor Converter

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Abstract—This paper presents the modeling & implementation of a closed-loop high-gain switched-inductor switched-capacitor converter (SISCC) for step-up DC-DC conversion & regulation. The power part of SISCC consists of two cascaded blocks: (i) Front: a serial-parallel switched-capacitor (SC) circuit with \(mc\) pumping capacitors, and (ii) Core: a switched-inductor (SI) booster with \(mc\) resonant capacitors, so as to boost the step-up gain up to \((mc+1)x(mc+1)\) at most, where \(D\) is the duty cycle of pulse-width-modulation (PWM) control. The control part of SISCC is composed of a phase generator and PWM controller, mainly implemented in the chip (I.C. number: D35-101B-37e, TSMC 0.35\mu M, size: 500\mu M \times 300\mu M, 12.2mW, max. frequency: 200kHz) via full-custom fabrication of National Chip Design and Implementation Center (CIC), Taiwan. Some theoretical analysis includes: formulation, steady-state analysis, and conversion ratio. Finally, the performance of this scheme is verified experimentally on a SISCC prototype, and the results are illustrated to show the efficacy of this scheme.

Index Terms—switched-inductor switched-capacitor converter, step-up, pulse-width-modulation, full-custom fabrication.

I. INTRODUCTION

A switched-capacitor converter (SCC), possessed of charge pump, is one of solutions to DC-DC power conversion because it has only semi-conductor switches and capacitors. Unlike traditional converters, the inductor-less SCC has a light weight & small volume. Up to now, many types have been suggested [1], and some well-known ones are listed below. In 1976, Dickson charge pump was proposed with a two-phase diode-capacitor chain [2], but its drawbacks are the fixed gain and large device area. In the 1990s, Ioinovici proposed a SCC with two symmetrical capacitor cells working at the anti-phase [3]. In 1997, Zhu and Ioinovici performed a comprehensive steady-state analysis of SCC [4]. In 2009, Tan et al. proposed the modeling and design of SCC by variable structure control [5]. In 2011, Chang proposed an integrated step-up/down SCC (SCVM/SCVD) [6]. However, these kinds of Ioinovici SCC have the gain just proportional to pumping capacitor count.

In 1991, Ueno proposed a SC transformer for step-up ratio of Fibonacci series [7]. However, this converter suffered from a limited line regulation. In 1997, Makowski suggested a two-phase canonical multiplier [8]. An \(n\)-stage Makowski charge pump has the gain limited by the \((n+1)\)-th Fibonacci number. In 2001, Starzyk presented a multiphase voltage doubler (MPVD) [9]. An \(n\)-stage MPVD has the gain of \(2^n\) at most, i.e. the capacitor count in Starzyk is fewer for the same gain. Nevertheless, some improving spaces still exist. Starzyk MPVD has the merits of fewer capacitor count and high gain, but it needs a complicated multiphase control circuit. Dickson charge pump or Ioinovici SCC has a simple two-phase control circuit, but the gain is proportional to capacitor count. In 2013, Chang and Kuo presented a four-phase serial-parallel SCC for a higher step-up gain like a multiplication which is the front stage number multiplied by the rear one [10], but there is quite a great number of switches used. In this paper, a new SISCC is proposed not only to reach a higher step-up gain under the fewer number of switches, but also to use a simpler control circuit implemented in a chip by full-custom fabrication.

II. CONFIGURATION OF SISCC

Fig.1 shows a closed-loop SISCC with power and control parts. As in the upper half of Fig.1, the power part contains (i) a serial-parallel SC circuit and (ii) a SI booster with resonant capacitors in cascade between supply \(V_s\) and output \(V_o\). For more details, the front SC contains \(n_c\) pumping capacitors \((C_1,\ldots,C_{n_c})\), \(n_c+1\) switches, and \(2n_c\) diodes. The SI booster has an inductor \(L\), \(m_c\) resonant capacitors \((C_{o1},\ldots,C_{o m_c})\), \(m_c-1\) switches, and \(2 m_c - 1\) diodes, filter capacitor \(C_L\), and load resistor \(R_L\). Here, assume each power switch has the same on-resistance \(r_T\), and each pumping capacitor has the same capacitance \(C\) \((C_1 = \ldots = C_m = C)\) with the same equivalent series resistance (ESR) \(r_C\). Similarly, the resonant capacitors have the same capacitance \(C_o\) \((C_{o1} = \ldots = C_{o m_c} = C_o)\). Each capacitor voltage in the front/core circuits can be treated identical and denoted by \(V_C\) / \(V_{C_o}\), respectively. As in the lower half of Fig.1, the control part contains PWM block and phase generator, mainly implemented in the chip. From the view of signal flow, \(V_o\) is fed back into low-pass filter (LPF) for high-frequency noise rejection, and then the filtered \(V_o\) is compared with reference input \(V_{ref}\) (i.e. desired output) to produce duty cycle \(D\) (via the PWM block) for keeping \(V_o\) on following \(V_{ref}\) to enhance output regulation as well as robustness against source/load variation.

To simplify the explanation, the operation of SISCC as \(n_c = 2, m_c = 2\) is discussed. Fig. 2 shows the theoretical waveforms within \(T_S\) \((T_S = 1/f_S, f_S: \text{switching frequency})\), where \(T_S\) contains three phases (Phase I, II, and III), and the phases have the different phase cycles as: \(x\cdot DT_S\), \((1-x)\cdot DT_S\), and \((1-D)T_S\), where \(x\) is the pre-charge cycle ratio (about 0.2 generally), and \(D(0 < D < 1)\) is the duty-cycle ratio of PWM. Based on the phase generator, the operations of Phase I, II, and III are scheduled as

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follows. (i) Phase I: turn on \( S_1 \) (driver signal: \( \phi_1 = 1 \)) and \( S_4 \) as in Fig. 3(a). \( C_1, C_2 \) are charged in parallel by \( V_S \) via \( S_4 \) and \( D_2 \) to raise the inductor current. At the same time, \( C_{o1}, C_{o2} \) are discharged in series via \( S_4 \) and \( D_4 \) to supply the load \( R_L \) and \( C_L \). (ii) Phase II: turn on \( S_2, S_3 \) (\( \phi_2 = 1 \)) and \( S_4 \) as in Fig. 3(b). \( C_1, C_2 \) are discharged in series together with \( V_S \) to form a higher voltage for charging \( L \) via \( S_4, S_3, S_2 \). \( C_{o1}, C_{o2} \) are still discharged in series to supply \( R_L \) and \( C_L \). (iii) Phase III: turn on \( S_2, S_3 \) (\( \phi_3 = 1 \)) as in Fig. 3(c). \( C_1, C_2 \) and \( L \) are discharged in series together with \( V_S \) via \( S_2, S_3 \) to transfer the stored energy into \( C_{o1}, C_{o2} \) in parallel via \( D_8, D_9 \). \( C_L \) stands alone to supply \( R_L \). Based on these scheduled operations cyclically, it is obvious that the front SC can provide \((2+1)\) times the voltage of \( V_S \) at most (\( \because n_c = 2 \)), and the SI booster with 2 resonant capacitors can provide the gain of \( 2/(1-D) \) (\( \because m_c = 2 \)). So, it stands to reason that the overall step-up gain can reach \((n_c+1)\times m_c/(1-D)\) at most.

III. FORMULATION OF SISCC

For the simplification, the Thevenin’s equivalence of the front SC circuit is taken, and then by combining this equivalent circuit with the core-stage SI booster, the overall modeling of SISCC can be formulated. Firstly, according to the Phase I, II, and III topologies as in Fig. 3(a)-(c), the open-circuit voltage \( V_{\text{open}} \) and resistance \( r_{\text{open}} \) of the front SC circuit can be easily found as:

\[
V_{\text{open}} = [ (n_c + 1) - n_c \cdot xD ] \cdot V_S - xD \cdot V_d , \quad (1a)
\]

\[
r_{\text{open}} = n_c \cdot (1 - xD) \cdot (r_1 + r_c) , \quad (1b)
\]

where \( V_d \) is the cut-in operating voltage of diodes. Next, via replacing the Thevenin’s equivalence of (1) into the SISCC, the equivalent topologies are obtained. Then based on these topologies, the dynamic equations for the PWM-ON and PWM-OFF periods can be derived. By using state-space averaging technique, the total state equation of SISCC can be derived as: ((\( \bullet \)) means \( d(\bullet)/dt \))

\[
x'(t) = A_u \cdot x(t) + B_u^{\text{act}} \cdot v(t) , \quad (2a)
\]

\[
y(t) = C_u \cdot x(t) , \quad (2b)
\]

where

Fig. 1. Configuration of SISCC.

Fig. 2. Theoretical waveforms of SISCC.
\[ V_o = \frac{1}{(n_i + 1)} \times \frac{m_c}{1 - D} \times \frac{n_i + 1}{1 + R_mR_L} \]

where \( k = V_d/V_S \) is the ratio of \( V_d \) to \( V_S \). When \( V_S = 5 \text{V} \) and \( V_d = 0.2 \text{V} \), the ratio is \( k = V_d/V_S = 0.04 \). For example, \( k = 0.04 \), \( x = 0.2 \), and \( R_L \gg r_T, r_C \) (\( R_L \) is in \( \Omega \)-level, and \( r_T, r_C \) is in \( m\Omega \)-level), \( M_o \) is really close to the theoretical maximum gain of \((n_i + 1) \times m_c / (1 - D)\). For nominal conditions, the maximum attainable value of \( V_o \) is \((n_i + 1) \times m_c / (1 - D) \times V_S\) minus voltage drops in the charging or discharging circuits.

IV. EXAMPLES OF SISCC

A closed-loop SISCC with \( n_i = 2, m_c = 2 \) is simulated by OrCAD, and its hardware circuit is implemented and tested. First, based on Fig. 1, the SISCC is designed to realize the step-up gain of \((2 + 1) \times 2 / (1 - 0.63) = 16.2\) (\( D = 0.63, x = 0.2 \)), and then this SISCC can boost \( V_o \) up to 81V at most (\( V_S = 5 \text{V}, R_L = 700 \Omega, f_S = 100 \text{kHz}, 27 \text{C} \)). The circuit parameters are listed as: \( L = 47 \mu\text{H}, C = 25 \mu\text{F}, C_o = 80 \mu\text{F}, C_L = 300 \mu\text{F}, r_C = 20 \text{m}\Omega, r_T = 30 \text{m}\Omega \). Besides, the hardware circuit is realized as photo shown in Fig. 4. There are two parts including: (i) SISCC (right: 14\text{cm} \times 10\text{cm}), (ii) phase generator and PWM controller (left: 14\text{cm} \times 10\text{cm}), mainly implemented in the circle-marked chip (LC No.: D35-101B-37e, TSMC 0.35\mu\text{m} 2P4M, size: 500\mu\text{m} \times 300\mu\text{m}, 12.2\text{mW}, max. frequency: 200kHz) via full-custom fabrication of National Chip Design and Implementation Center, Taiwan. Fig. 5 shows the layout and wire-bonding diagrams of D35-101B-37e. The simulation results of \( V_o \) and output ripple for \( V_{\text{ref}} = 80\text{V} \) are shown in Fig. 6(a)-(b), and the waveforms of capacitor voltage
and inductor current are shown in Fig. 6(c). Obviously, the converter is stable to keep \( V_o \) following \( V_{ref} \). The settling time is shorter than 20ms, and the ripple percentage is about 0.05%. The experiment results of \( V_o \) for \( V_{ref} = 80\text{V}, 75\text{V} \) are shown in Fig. 7(a)-(b). Obviously, \( V_o \) has the steady-state value of about 80.19\text{V}, 75.05\text{V}, and is following \( V_{ref} = 80\text{V}, 75\text{V} \) via the controller chip.

V. CONCLUSIONS

This paper presents the modeling & implementation of a closed-loop high-gain SISCC for step-up DC-DC conversion & regulation. The power part consists of two cascaded blocks: a serial-parallel SC circuit with \( n_p \) pumping capacitors and a SI booster with \( m_r \) resonant capacitors, so as to obtain a high step-up gain of \((n_p + 1)\times m_r/(1-D)\) at most, where \( D \) is the duty cycle of PWM. The control part consists of a phase generator and PWM controller, mainly implemented in the chip via full-custom fabrication (TSMC 0.35\text{um} 2P4M). Finally, the performance of this scheme is verified experimentally on a SISCC prototype, and the results are illustrated to show the efficacy of this scheme.

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