A Switch-Utilization-Improved Switched-Inductor Switched-Capacitor Converter with Adapting Stage Number

(Short title: A Switch-Utilization-Improved SISCC with Adapting Stage Number)

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Abstract: A novel closed-loop switched-inductor switched-capacitor converter (SISCC) is proposed by using the pulse-width-modulation (PWM) compensation for the step-up DC-DC conversion/regulation, and by combining the adaptive-stage-number (ASN) control for the higher switch utilization and wider supply range. The power part of SISCC is composed of two cascaded sub-circuits, including (i) a serial-parallel switched-capacitor circuit with $n_c$ pumping capacitors, and (ii) a switched-inductor booster with $m_c$ resonant capacitors, so as to obtain the step-up gain of $(n_c+1) \times \frac{m_c}{(1-D)}$ at most, where $D$ is the duty cycle of PWM adopted to enhance output regulation as well as robustness to source/loading variation. Further, the ASN control is presented with adapting the stage number $n$ ($n=1,2,\ldots,n_c$) of pumping capacitors to realize a flexible gain of $(n+1) \times \frac{m_c}{(1-D)}$, and with combining supply voltage and desired output to obtain a properly small duty cycle $D$ for improving switch utilization and/or supply voltage range. Some theoretical analysis and control design include: formulation, steady-state analysis, ASN-based conversion ratio, efficiency, output ripple, stability, inductance and capacitance selection, and control design. Finally, the performance of this scheme is verified experimentally on an ASN-based SISCC prototype, and all results are illustrated to show the efficacy of this scheme.

Keywords: switched-inductor, switched-capacitor, step-up converter, switch utilization, adaptive-stage-number (ASN), pulse-width-modulation (PWM).

1. Introduction

The switched-capacitor converter (SCC), possessed of the charge pump structure, is one of solutions to DC-DC power conversion because it has only semi-conductor switches and capacitors. Unlike traditional converters, the inductor-less SCC has a light weight and a small volume. Up to now, many types have been suggested [1], and some well-known topologies are listed as: (i) Dickson, (ii) Ioinovici, (iii) Ueno, and (iv) Makowski charge pump or SCC. In 1976, Dickson charge pump was proposed with a two-phase diode-capacitor chain [2-3], but it has the drawbacks of the fixed gain and large device area. In the 1990s, Ioinovici proposed a SCC with two symmetrical capacitor cells, and presented a current-mode SCC [4-5]. In 1997, Zhu and Ioinovici performed a comprehensive steady-state analysis of SCC [6]. In 2009, Tan et al. proposed the modeling and design of SCC by variable structure control [7]. In 2010, Chang presented a generalized $n$-stage current-mode multiphase SCC [8-9]. In 2011, Chang proposed a new integrated type of step-up/down SCC (SCVM/SCVD) [10]. However, these kinds of Ioinovici SCC have the gain just proportional to the number of pumping capacitors.

In 1991, Ueno proposed a SC transformer for step-up ratio of Fibonacci series, as well as low-ripple SCC [11-12]. However, these converters suffered from a limited line regulation. In 1997, Makowski suggested a two-phase canonical multiplier [13]. An $n$-stage Makowski charge pump has the gain limited by the $(n+1)$-th Fibonacci number [14-15]. In 2001, Starzyk presented a multiphase voltage doubler (MPVD) [16]. An $n$-stage MPVD has the gain of $2^n$ at most [17], i.e. the capacitor count in Starzyk is fewer for the same gain. Nevertheless, some improving spaces still exist. (i) Starzyk MPVD has the merits of fewer capacitor count and high gain, but it needs a complicated multiphase control circuit. Dickson charge pump or Ioinovici SCC has a simple two-phase control circuit, but the gain is proportional to capacitor count. In 2013, Chang and Kuo presented a four-phase serial-parallel SCC to obtain a high
step-up gain value which is the front stage number multiplied by the rear one [18], but there are quite many number of semi-conductor switches used. In this paper, a new SISCC is proposed not only to reach a higher step-up gain under the fewer number of switches, but also to use a simpler control circuit for a three-phase operation. (ii) When a higher step-up gain is required in the conventional booster, a bigger duty cycle is needed for this high gain. It often results in switch utilization degradation. Here, the ASN control is suggested by changing the stage number flexibly to operate this SISCC at a properly small duty cycle for improving switch utilization and/or supply range. This idea by adapting stage number is not completely new. Recently, many researchers utilized this idea for realizing an efficiency-enhanced converter [19-20]. Here, we take the first lead in proposing a new scheme of SISCC, and combining ASN and PWM control for the switch-utilization-improved conversion and regulation.

2. Configuration of ASN-Based SISCC

Fig. 1 shows a closed-loop scheme of ASN-based SISCC with power and control parts. As in the upper half of Fig. 1, the power part is composed of two sub-circuits, including (i) Front: a serial-parallel SC circuit and (ii) Rear: a SI booster with resonant capacitors, connected in cascade between supply $V_S$ and output $V_o$. For more details, the front SC circuit contains $n_c$ pumping capacitors ($C_1,\ldots,C_{n_c}$), $n_c + 1$ power switches, and $2n_c$ diodes. The core SI booster has one inductor $L$, $m_c$ resonant capacitors ($C_{o1},\ldots,C_{om_c}$), $m_c - 1$ power switches, $2m_c - 1$ diodes, filter capacitor $C_L$, and load resistor $R_L$. Here, assume each power switch has the same on-resistance $r_T$, and each pumping capacitor has the same capacitance $C$ ($C_1 = \ldots = C_{n_c} = C$) with the same equivalent series resistance (ESR) $r_C$. Similarly, the resonant capacitors are with the same capacitance $C_o$ ($C_{o1} = \ldots = C_{om_c} = C_o$). Thus, each capacitor voltage in the front and rear sub-circuits can be treated identical and denoted by $v_C$ and $v_{C_o}$, respectively.

As in the lower half of Fig. 1, the control part is composed of PWM compensator, ASN decision, and ASN phase generator. By adopting the PWM compensator, the regulation capability can be enhanced to keep $V_o$ on following desired output $V_{\text{ref}}$ (reference), and so can robustness to source/loading variation. By using the ASN control, the switch utilization can be improved to reduce the current/voltage stress on switch $S_x$, and so can supply voltage range. In this paper, assume that the discussions (formulation, theoretical analysis and design) are based on circuit-level aspect, not based on layout physical level. Thus, parasitic elements are assumed small enough to be neglected here.

2.1 Power Part—SISCC:

For the simplification of explanation, the number of pumping and resonant capacitors are temporarily assumed at $n_c = 2$, $m_c = 2$. Here, the “running” stage number $n$ of the front SC circuit is no more than 2 ($n = 0, 1, \text{or } 2$). Now, the operation of SISCC as running $n = 2$ is discussed. Fig. 2 shows the theoretical waveforms within $T_S$ ($T_S = 1/f_S$, $f_S$: switching frequency), where $T_S$ contains three phases (Phase I, II, and III), and each phase has the different phase cycle. Phase I, II, and III has the phase cycle of $x \cdot DT_S$, $(1-x) \cdot DT_S$, and $(1-D)T_S$ respectively, where $x$ represents the pre-charge cycle ratio taken at about 0.2 generally, and $D$ ($0 < D < 1$) is the duty-cycle ratio of PWM. The operations of Phase I, II, and III are explained as follows. (i) Phase I: turn on $S_0$ (driver signal: $\phi_1 = 1$) and $S_y$ as topology in Fig. 3(a). $C_1C_2$ are charged in parallel by $V_S$ via $S_0$ and diodes $D_1 - D_4$, and $L$
is charged by \( V_S \) via \( S_p \) and \( D_2 \) to raise the inductor current. At the same time, \( C_{o1}, C_{o2} \) are discharged in series via \( S_r \) and \( D_I \) to supply the load \( R_L \) and \( C_L \). (ii) Phase II: turn on \( S_1, S_2 \) (driver signal: \( \phi_2 = 1 \)) and \( S_r \) as in Fig. 3(b). \( C_1, C_2 \) are discharged in series together with \( V_S \) to form a higher voltage for charging \( L \) via \( S_1, S_2, S_r \). Simultaneously, \( C_{o1}, C_{o2} \) are still discharged in series to supply \( R_L \) and \( C_L \). (iii) Phase III: turn on \( S_1, S_2 \) (driver signal: \( \phi_2 = 1 \)) as in Fig. 3(c). \( C_1, C_2 \) and \( L \) are discharged in series together with \( V_S \) via \( S_1, S_2 \) to transfer the stored energy into \( C_{o1}, C_{o2} \) in parallel via \( D_3, D_6 \). Then, the filter capacitor \( C_L \) stands alone to supply the load \( R_L \).

Based on these scheduled operations cyclically, it is obvious that the front SC circuit can provide \((2+1)\) times the voltage of supply \( V_S \) at most \((\therefore n_c = 2)\), and the rear SI booster with 2 resonant capacitors can provide the voltage gain of \( 2/(1-D) \) in the CCM theoretically \((\therefore m_c = 2)\). Thus, it stands to reason that the total step-up gain can reach \((n_c+1 \times m_c)/(1-D) \) at most, where \( D \) is the duty cycle of PWM.

2.2 Control Part—PWM and ASN:

The control part as in the lower half of Fig. 1 is composed of PWM compensator, ASN decision, and ASN phase generator. Firstly, from the view of signal flow, \( V_o \) is fed back into the low-pass filter (LPF) for high-frequency noise rejection, and then the filtered \( V_o \) is compared with reference \( V_{\text{ref}} \) (i.e. desired output) to produce a duty-cycle \( D \) via the PWM compensator. By using this signal \( D \), switch \( S_r \) is controlled to keep \( V_o \) on following \( V_{\text{ref}} \) so as to enhance output regulation as well as robustness against source/loading variation.

Secondly, from the view of switch utilization, a conventional booster has the step-up gain of \( 1/(1-D) \) theoretically in the CCM mode. A bigger duty cycle \( D \) leads the higher step-up gain, but it results in the lower switch utilization. Here, the switch utilization is defined by \( P_s/P_T \), where \( P_s \) is the rated output power of this booster and \( P_T \) is the product of the voltage and current peaks of switch \( S_r \). In other words, the high gain in this kind of booster easily causes the low switch utilization, i.e. large voltage/current peaks on switch \( S_r \), especially for the higher step-up gain. In this ASN-based SISCC, the gain is \((n+1) \times m_c/(1-D), \ n = 0,1,2,...,n_c \) theoretically. For one step-up gain (\( V_{\text{ref}} \) and \( V_S \) assigned), it is feasible that ones can use a properly small duty cycle \( D \) with the help of adapting a bigger stage number \( n \) for this given gain. Then, the switch utilization can be improved with this ASN, i.e. to reduce the voltage/current stress on power switch. For achieving this idea, there are two units as in the lower half of Fig. 1 described as follows. (i) ASN Decision Unit: This unit is able to choose a running stage number \( n \) according to \( V_{\text{ref}} \) and \( V_S \) to make duty cycle \( D \) smaller properly, i.e. via adapting \( n \) \((n = 0,1,2,...,n_c)\) to minimize \( D \) subject to \( D \geq D_{\text{min}}, \ \min [1-(n+1) \times m_c \cdot V_S/V_{\text{ref}}] \geq D_{\text{min}}, \) where \( D_{\text{min}} \) is the reasonable smallest duty cycle. The too small duty cycle of PWM will cause the difficulties of realization of very short duration as well as weaker regulation capability. (ii) ASN Phase Generator Unit: Based on this \( n \), this generator can generate the driver signals of \( S_0, S_1, S_2, \ldots \) to manipulate the topological path and together with \( D \) of PWM for this gain level.

3. Formulation of ASN-Based SISCC

In this section, the formulation of ASN-based SISCC is derived, and it will be helpful to the theoretical analysis and design later. For the simplification, the Thevenin’s equivalence of the front-stage SC sub-circuit is taken, and then
by combining this equivalent circuit with the rear-stage SI booster, the overall modeling of SISCC can be formulated. Firstly, according to the Phase I, II, and III topologies as in Fig. 3(a)-(c), the open-circuit voltage $V_{open}$ and resistance $r_{open}$ of the front-stage SC as running stage number $n$ can be found as: (i) Phase I: $V_{open} = V_S - V_d$, $r_{open} = 0$ ($V_d$: on-state voltage of diodes); (ii) Phase II: $V_{open} = V_S + n \cdot v_C$, $r_{open} = n \cdot (r_T + r_C)$; (iii) Phase III: $V_{open} = V_S + n \cdot v_C$, $r_{open} = n \cdot (r_T + r_C)$, $n = 0, 1, 2, ..., n_c$. Here, this SC sub-circuit mainly plays for a role of a pre-stage booster to make $V_{open}$ towards to the goal of $(n+1)$ times voltage of $V_S$, so it can be assumed that the response of the front-stage SC is much faster than that of the rear-stage SI booster. Thus, it is reasonable that the derivation of the pumping capacitor voltage is near to zero after entering steady state of SISCC, i.e. $v_C' = 0$, $v_C \approx V_S$.

Based on this assumption plus the state-space averaging (SSA), $V_{open}$ and $r_{open}$ of this SC sub-circuit as running stage number $n$ can be obtained as:

$$V_{open} = xD - (V_S - V_d) + (1-x)D \cdot (V_S + n \cdot V_S) + (1-D) \cdot (V_S + n \cdot V_S) = [(n+1) - n \cdot xD] \cdot V_S - xD \cdot V_d,$$

$$r_{open} = xD \cdot 0 + (1-x)D \cdot n \cdot (r_T + r_C) + (1-D) \cdot n \cdot (r_T + r_C) = n \cdot (1-xD) \cdot (r_T + r_C).$$

Next, via replacing the Thevenin’s equivalence of (1) into the SISCC, the overall topologies for the PWM-ON and PWM-OFF periods can be obtained as in Fig. 4(a) and 4(b), respectively. Based on the topologies, the relevant dynamic equations are derived as follows.

(i) PWM-ON period: within $D \cdot T_S$ (Fig. 4(a))

$$\frac{d[i_L(t)]}{dt} = -\frac{R_A}{L} \cdot i_L(t) + \frac{1}{L} \cdot V_{open},$$

$$\frac{d[v_{C_o}(t)]}{dt} = -\frac{m_c}{C_o R_B} v_{C_o}(t) + \frac{1}{C_o R_B} v_{C_L}(t) + \frac{1}{C_o R_B} V_d,$$  

$$\frac{d[v_{C_L}(t)]}{dt} = \frac{m_c}{C_L R_B} v_{C_o}(t) - \frac{1}{C_L} \left( \frac{1}{R_B} + \frac{1}{R_L} \right) v_{C_L} - \frac{1}{C_L R_B} V_d,$$  

$$v_o(t) = v_{C_L}(t), \quad i_S(t) = i_L(t),$$  

(ii) PWM-OFF period: within $(1-D) \cdot T_S$ (Fig. 4(b))

$$\frac{d[i_L(t)]}{dt} = -\frac{R_C}{L} \cdot i_L(t) - \frac{1}{L} \cdot v_{C_o}(t) + \frac{1}{L} \cdot V_{open} - \frac{1}{L} \cdot V_d,$$  

$$\frac{d[v_{C_o}(t)]}{dt} = \frac{1}{m_c C_o} \cdot i_L(t),$$  

$$\frac{d[v_{C_L}(t)]}{dt} = -\frac{1}{C_L R_L} v_{C_L},$$  

$$v_o(t) = v_{C_L}(t), \quad i_S(t) = i_L(t),$$

where $R_A = r_{open} + r_L + r_T$, $R_B = (m_c-1) \cdot r_T + m_c \cdot r_C$, $R_C = r_{open} + r_L + r_C / m_c$ are the parasitic resistances, $v_o(t)$ is the output voltage, and $i_S(t)$ is the current passing through $V_{open}$. Again by using SSA technique, the state equation of ASN-based SISCC can be derived as: ((●)’ means $d(●)/dt$)

$$x'(t) = A_n \cdot x(t) + B_a \cdot u(t),$$  

$$y(t) = C_n \cdot x(t),$$

where

$$x(t) = [v_{C_o}(t) \ v_{C_L}(t) \ V_d]^T, \quad u(t) = [V_{open} \ V_d]^T, \quad y(t) = [v_o(t) \ i_S(t)]^T,$$
\[
A_d = \begin{bmatrix}
\frac{R_D}{L} & 1 - D & 0 \\
\frac{1 - D}{m_c R_C} & \frac{D}{m_c R_C} & 0 \\
0 & \frac{1}{C_L R_C} & \frac{D}{C_L R_C + \frac{1}{C_L}}
\end{bmatrix}, \quad B_d = \begin{bmatrix}
\frac{1}{L} & 1 - D & 0 \\
0 & \frac{D}{C_p R_B} & 0 \\
0 & \frac{-m_c D}{C_L R_B}
\end{bmatrix}, \quad C_n = \begin{bmatrix}
0 & 0 & 1 \\
1 & 0 & 0
\end{bmatrix}.
\]

\[R_D = r_{open} + r_L + D \cdot r_T + (1 - D) \cdot r_C / m_c .\]  

(5g)

4. Analysis and Design of ASN-Based SISCC

4.1 Conversion Ratio and Power Efficiency:

By substituting \( x'(t) = 0 \) of (4), the steady-state output voltage \( V_o \), output current \( I_o \), and supply-terminal current \( I_S \) can be obtained as:

\[V_o = -C_{n_1} \cdot A_d^{-1} \cdot B_d \cdot u = \frac{m_c}{1 - D} \cdot \left[ \frac{(n+1) \cdot n \cdot D - V_S \cdot \left[ xD + (1 - D) \cdot (m_c + 1)/m_c \right]}{1 + R_o / R_L} \right], \quad I_o = \frac{V_o}{R_o} , \]

\[I_S = -C_{n_2} \cdot A_d^{-1} \cdot B_d \cdot u = m_c \cdot \frac{(n+1) \cdot n \cdot D - V_S \cdot \left[ xD + (1 - D) \cdot (m_c + 1)/m_c \right]}{1 + R_o / R_L} . \]

where

\[R_o = \frac{R_B}{D} \cdot \frac{m_c^2 \cdot R_D}{(1 - D)^2} . \]

\[C_{n_1} = [0 \quad 0 \quad 1] , \quad C_{n_2} = [1 \quad 0 \quad 0] . \]

From (6a), it is obvious that \( V_o \) can be regulated by duty cycle \( D \), and then the step-up voltage conversion ratio is suggested as

\[M_n = \frac{V_o}{V_S} = (n+1) \cdot \frac{m_c}{1 - D} \cdot \left( 1 - \frac{n \cdot D + \left( xD + (1 - D) \cdot (m_c + 1)/m_c \right) \cdot k}{n+1} \right) \cdot \left[ \frac{1 + R_o}{R_L} \right] , \]

where \( k = V_d / V_S \) is the ratio of \( V_d \) to \( V_S \). When \( V_S = 5V \) and \( V_d = 0.2V \), the ratio is \( k = V_d / V_S = 0.04 \). For example, \( k = 0.04 \), \( x = 0.2 \), and \( R_L >> r_T, r_C \) (\( R_L \) is in \( \Omega \)-level, and \( r_T, r_C \) is in \( m\Omega \)-level, i.e. \( R_L >> R_a \)).

\( M_n \) is really close to the theoretical value of \( (n+1) \cdot m_c / (1 - D) \), \( n = 0, 1, 2, ..., n_c \). Thus, the ideal maximum gain is \( (n_c + 1) \cdot m_c / (1 - D) \). For nominal conditions, the maximum attainable value of \( V_o \) is \( \left[ (n+1) \cdot m_c / (1 - D) \right] \cdot V_S \) minus voltage drops in the charging or discharging circuits. Next, according to Fig. 4, the input and output power can be computed as

\[P_i = V_{open} \cdot I_S , \quad P_o = V_o \cdot I_o / R_L . \]

(9a,b)

According to (9) plus (6) and (1a), the power efficiency of ASN-based SISCC is derived as in (10). Clearly, \( \eta_n \) is rising when \( V_o \) (i.e. \( V_{ref} \)) is closer to \( \left[ (n+1) \cdot m_c / (1 - D) \right] \cdot V_S \).

\[\eta_n = \frac{P_o}{P_i} = \frac{V_o / V_s}{\left[ (n+1) \cdot m_c / (1 - D) \right]} \cdot \frac{1}{\left[ (n+1) \cdot m_c / (1 - D) \right]} \cdot V_o . \]

(10)

Here, let’s discuss the benefit to switch utilization and supply range by using ASN. For example, \( V_S = 5V \), \( V_{ref} = 50V \), and the total step-up gain is \( V_{ref} / V_S = 50 / 5 = 10 \). If \( n = 0 \), \( D \) will be 0.8 for this gain (’step-up gain = (0+1) \cdot 2 / (1-0.8) = 10’). If \( n = 1 \), \( D \) will be 0.6 (’step-up gain = (1+1) \cdot 2 / (1-0.6) = 10’). If \( n = 2 \) is adapted, then \( D \) needs just 0.4. (’step-up gain = (2+1) \cdot 2 / (1-0.4) = 10’). Obviously, based on ASN, \( n \)
\((n = 0,1,2,\ldots,n_c)\) can be adapted according to \(V_S\) and \(V_{\text{ref}}\) to use a smaller duty cycle \(D\) for the higher switch utilization. Besides, the range of the total gain can be extended with ASN. It is helpful that the SISCC has the wider range of supply \(V_S\) when \(V_{\text{ref}}\) is given. For example, assume that \(V_S\) is 5V normally and decreasing along with time, \(V_o\) (i.e. \(V_{\text{ref}}\)) is desired at 50V, \(m_c = 2\), \(k = 0.04\), \(x = 0.2\), and \(D = 0.10 - 0.82\) \((D_{\min} = 0.1)\). If \(n = 0\), \(V_S\) needs 4.5V at least or above. If \(n = 1\), \(V_S\) needs 2.25V or above. If \(n = 2\) is adapted, the SISCC will still work as \(V_S\) needs just 1.5V or above. The range of supply voltage becomes wider by using ASN. Certainly, ones might pay a price of power consumption due to using the bigger stage number of the front-stage SC.

4.2 Inductance/Capacitance Selection:

(i) Selection of inductor \(L\):

Based on the theoretical waveform of inductor current of Fig.2, plus the topologies of Fig. 3(a)-(c), the relationship of Phase I, II, III referring to the inductance can be simplified and presented as:

\[
t_1 = L \cdot \frac{I_2 - I_1}{V_S} = x \cdot D T_S, \quad t_2 = L \cdot \frac{I_3 - I_2}{V_S} = (1 - x) \cdot D T_S, \quad t_3 = L \cdot \frac{I_3 - I_1}{V_o - (n+1) \cdot V_S} = (1 - D) T_S. \quad (11a,b,c)
\]

By adding (11a), (11b), and (11c), the sum of the three phase cycles is obtained as

\[
t_1 + t_2 + t_3 = \frac{L \cdot \Delta I}{V_S} \cdot \frac{1}{D (n+1-x-n)} = T_S = \frac{1}{f_S}, \quad (12)
\]

where \(\Delta I = I_3 - I_1\) is denoted by the current swing of inductor \(L\). According to (12), the minimum inductance for a current swing \(\Delta I\) can be estimated as in (13). Certainly, if ones desire a smaller \(\Delta I\), the inductor \(L\) will be larger, but it is improved by increasing \(f_S\).

\[
L \geq L_{\min} = \frac{DV_S \cdot (n+1-x-n)}{f_S \cdot \Delta I}. \quad (13)
\]

(ii) Selection of pumping capacitor \(C\):

Based on the topology of Phase I as in Fig. 3(a), \(\tau_1\) must be smaller than \(x \cdot D T_S\) for the fast response, where \(\tau_1\) is the time constant of charging these pumping capacitors from supply \(V_S\), and the inequality is presented as in (14). Obviously, \(C\) should be selected as smaller for the fast boosting response of the front-stage SC.

\[
\tau_1 = n \cdot C \cdot (\tau_T + \frac{k}{n}) < x \cdot D T_S. \quad (14)
\]

(iii) Selection of filter capacitor \(C_L\):

As in Fig. 2, \(v_o\) decays from \(V_{o,1}\) to \(V_{o,2}\) exponentially in Phase II, and then decays from \(V_{o,2}\) to \(V_{o,3}\) exponentially in Phase III. Thus, \(v_o\) can be modeled as

\[
v_o(t) = \begin{cases}
V_{o,1} \cdot e^{-(t/T_2)}, & 0 \leq t \leq (1-x) \cdot D T_S \quad \text{[Phase II]} \\
V_{o,2} \cdot e^{-(t/T_3)}, & 0 \leq t \leq (1-D) \cdot T_S \quad \text{[Phase III]} 
\end{cases}
\]

where \(V_{o,2} = V_{o,1} \cdot e^{-(x \cdot D T_S)/T_2}\), \(V_{o,3} = V_{o,2} \cdot e^{-(1-D) T_S/T_3}\), and the discharging time constants of Phase II and III are \(\tau_2 = R_L \cdot (C_L + C_o/m_c)\), \(\tau_3 = R_L \cdot C_L\), respectively. So, the voltage ripples can be defined as

\[
\Delta V_{o,II} = V_{o,1} - V_{o,2} = V_{o,1} \cdot [1 - e^{-(1-x) \cdot D T_S/T_2}],
\]

\[
\Delta V_{o,III} = V_{o,2} - V_{o,3} = V_{o,2} \cdot [1 - e^{-(1-D) T_S/T_3}]. \quad (16a,b)
\]

By using (15)-(16), plus assuming \(C_L > C_o\), the averaged output voltage can be derived as
\[
V_o = \frac{1}{(1-xD)T_S} \int_{0}^{(1-xD)T_S} v_o(t) \, dt = \frac{R_L}{(1-xD)T_S} \left[ C_L (\Delta V_{o,II} + \Delta V_{o,III}) + \frac{C_o}{m_c} \Delta V_{II} \right] = \frac{R_L C_L}{(1-xD)T_S} \Delta V_o,
\]

where \( \Delta V_o = \Delta V_{o,II} + \Delta V_{o,III} \) is the total swing of output voltage. Then, the ripple percentage can be presented as

\[
\eta_p = \frac{\Delta V_o}{V_o} = \frac{1-xD}{R_L C_L} = \frac{1-xD}{f_S \cdot R_L \cdot C_L}.
\]

Clearly, \( \eta_p \) is worse while the loading is heavier, but it is improved by increasing \( f_S \) or \( C_L \). When the converter is unloaded, \( \eta_p \) is almost zero. For a desired ripple \( \eta_p \), the filter capacitor is estimated as

\[
C_L \geq C_{L,\text{min}} = \frac{1-xD}{f_S \cdot R_L \cdot \eta_p}.
\]

### 4.3 Stability and PWM Control:

As in (5d), the system matrix \( A_n \) is divided into four sub-matrices \( A_{n1}, A_{n2}, A_{n1}, A_{n2} \), and then can be decomposed as in (20a), where diagonal matrix \( \Delta_n \) is computed as in (20b). Obviously, \( \Delta_n \) represents one of the characteristic roots of SISCC:

\[
A_n = \begin{bmatrix} A_{n1} & A_{n2} \\ A_{n1} & A_{n2} \end{bmatrix} = \begin{bmatrix} I & 0 \\ 0 & \Delta_n \end{bmatrix} \begin{bmatrix} A_{n1} & A_{n2} \\ A_{n1} & A_{n2} \end{bmatrix},
\]

\[
\Delta_n = A_{n2} - A_{n1} = -\frac{1}{C_L} \left( \frac{1}{R_o} + \frac{1}{R_0} \right).
\]

Based on this \( \Delta_n \), plus taking the resonant capacitor \( C_o = L(1-D)^2/(m_c R_D^2) \), the characteristic equation of the open-loop SISCC can be decomposed approximately as in (21), and then the characteristic roots \( p_1, p_2, p_3 \) can be obtained as in (22).

\[
\Delta(s) = [sI - A_n] = \left[ s + \frac{1}{C_L(R_L + R_o)} \right] \left[ s^2 + \left( \frac{R_0}{L} + \frac{m_c D}{C_L R_0} + \frac{1}{C_1 R_0 (1-D)^2 R_0} \right) s + \frac{D(1-D)^2 R_o}{m_c C_L R_0} \right] = \left( s - p_1 \right) \left( s - p_2 \right) \left( s - p_3 \right) = 0,
\]

where

\[
p_1 = -\frac{1}{C_L(R_L + R_o)},
\]

\[
p_2, p_3 = \left[ \frac{1}{2} \left( \frac{R_0}{C_L R_0} + \frac{m_c D}{C_L R_0 (1-D)^2 R_0} \right) \pm \sqrt{\left( \frac{R_0}{C_L R_0} + \frac{m_c D}{C_L R_0 (1-D)^2 R_0} \right)^2 - \frac{4}{C_1 R_0 (1-D)^2 R_0} \frac{D(1-D)^2 R_o}{m_c C_L R_0} } \right] / \frac{1}{C_1 R_0 (1-D)^2 R_0},
\]

when

\[
c_o = L(1-D)^2/m_c R_D^2.
\]

Obviously, the three different real roots: \( p_1, p_2, p_3 \) are all located in the left half of s-plane. Hence, the open-loop SISCC has an inherent good stability. Further, based on (8), \( R_L \) is much larger than \( R_o \) for the better voltage conversion ratio, i.e. \( R_L >> R_o > R_B \) (10 times larger or above). Based on (19), \( C_L \) is taken as larger for the smaller output ripple. In general, \( C_L \) is times larger than \( C_o \), i.e. \( C_L > C_o \). Because \( R_L >> R_o > R_B \) and \( C_L > C_o \), it concludes that \( |p_1| << |p_2|, |p_3| \), i.e. \( |p_1| \) is at least 10 times smaller than \( |p_2|, |p_3| \). Thus, \( p_1 \) as in (22a) is the dominant pole of SISCC, and its first-order approximation will be applied for the PWM control design.

As controller in Fig. 1, \( V_o \) is fed back into LPF for noise rejection, where \( \omega_L \) is a cut-off frequency chosen based on what range the noises occur at. To avoid affecting system response, \( \omega_L \) is taken as bigger than the inverse value of dominant pole \( p_1 \) (\( \omega_L > 1/|p_1| \)). Fig. 5 shows the closed-loop control diagram of ASN-based SISCC. If \( V_S \) or \( R_L \) is decreasing (source/loading variation), based on (6a), then \( V_o \) will be going down. The error \( e \) between \( V_{\text{ref}} \) and \( V_o \) is rising quickly. The bigger \( e \) makes a larger duty cycle \( D \) via \( K_P \) (proportional gain of PWM
control), and then this \( D \) will drive \( V_o \) to keep following \( V_{ref} \). The capability of output regulation (line/load regularity) is enhanced. Next, the design of \( K_P \) is discussed. Assume that the SISCC is running around a duty cycle \( D = D_o \) for \( V_o = V_{ref} \). With the help of taking these small \( k \) and \( x \), \( V_o \) of (6a) can be simplified as

\[
V_o = (n+1) \frac{m_c \cdot V_S}{1 - D_o} \cdot \frac{1}{1 + R_o/R_L}, \quad \text{for} \quad D = D_o.
\]  

(23)

If a small duty-cycle variation \( d \) occurs, the output voltage for \( D = D_o + d \) has a small change \( v_o \) as

\[
V_o + v_o = (n+1) \frac{m_c \cdot V_S}{1 - (D_o + d)} \cdot \frac{1}{1 + R_o/R_L}, \quad \text{for} \quad D = D_o + d.
\]  

(24)

By subtracting (23) from (24), and then combining the dominant pole \( p_1 \), the small-signal output voltage can be expressed with the s-domain first-order approximated model as:

\[
v_o(s) = \frac{(n+1) \cdot m_c \cdot V_S}{(1-D_o)^2} \cdot \frac{1}{1 + R_o/R_L} \cdot \frac{1}{\tau_1 \cdot s + 1} \cdot d(s),
\]  

where \( \tau_1 = \frac{1}{|p_1|} = C_L \cdot (R_L || R_o) \) is the small-signal time constant of SISCC. When we consider the response just at the frequency lower than \( \omega_L \) of LPF, based on Fig. 5 plus (25), the closed-loop characteristic equation is derived as

\[
\Delta c(s) = 1 + H(s) = 1 + K_P \cdot \frac{(n+1) \cdot m_c \cdot V_S}{(1-D_o)^2} \cdot \frac{1}{1 + R_o/R_L} \cdot \frac{1}{\tau_1 \cdot s + 1} = 0.
\]  

(26)

The closed-loop settling time \( t_S \) within a settling error of \( \pm 5\% \) is obtained as

\[
t_S = 3 \cdot \tau_1 \left[ 1 + K_P \cdot \frac{(n+1) \cdot m_c \cdot V_S}{(1-D_o)^2} \cdot \frac{1}{1 + R_o/R_L} \right].
\]  

(27)

For keeping \( t_S \) shorter than a desired settling time \( \tilde{t}_S \), the minimum gain of \( K_P \) can be designed as

\[
K_P \geq \frac{(1-D_o)^2 \cdot (R_L + R_o)}{(n+1) \cdot m_c \cdot V_S \cdot R_L} \left( \frac{3 \cdot \tau_1}{\tilde{t}_S} - 1 \right), \quad n = 0, 1, 2, \ldots, n_c.
\]  

(28)

Next, let the phase margin be higher than some desired \( \theta_d \) as \( PM = 180^\circ + \angle H(j \omega_g) > \theta_d \), where \( \omega_g \) is the gain-crossover frequency of \( H(s) \) (i.e. \( |H(j \omega_g)| = 1 \)). So, \( \omega_g \) is obtained as

\[
\omega_g = \frac{1}{\tau_1} \left[ \sqrt{K_P \cdot \frac{(n+1) \cdot m_c \cdot V_S}{(1-D_o)^2} \cdot \frac{1}{1 + R_o/R_L}} \right]^2 - 1.
\]  

(29)

By substituting (29) into the \( PM \) inequality, the maximum gain of \( K_P \) for \( \theta_d \) can be derived as

\[
K_P \leq \frac{(1-D_o)^2 \cdot (R_L + R_o)}{(n+1) \cdot m_c \cdot V_S \cdot R_L} \cdot \sec(\theta_d), \quad n = 0, 1, 2, \ldots, n_c.
\]  

(30)

5. Examples of ASN-Based SISCC

A closed-loop ASN-based SISCC (\( n_e = 2, m_e = 2 \)) is simulated by OrCAD, and then its hardware circuit is implemented and tested. Basically, the step-up conversion is to realize the gain of \((2+1) \times 2/(1-0.63) = 16.2\) (\( D = 0.63 \), \( x = 0.2 \), \( k = 0.04 \)), and then to boost the output voltage \( V_o \) into 81V at most (\( V_S = 5V \), \( R_L = 500\Omega \), \( f_S = 100kHz \)). By using (14), \( C \) is selected at \( 25\mu F \) (\( r_C = 20m\Omega \), \( r_T = 30m\Omega \)). According to (19), \( C_L \) is selected at \( 300\mu F \) for the desired ripple \( r^2 = 0.08\% \). According to (13), \( L \) is designed as \( 47\mu H \) for the current swing \( \Delta I = 2.0A \), and then following to take \( C_g \) of \( 80\mu F \) based on (22b). For noise rejection, \( \omega_L \) is taken by about \( 1000Hz \) here. Based on (28),(30), plus the larger duty cycle running in the transient response, \( K_P \) is basically
designed at 0.003 for $\bar{\tau}_S = 20\text{ms}$, $\theta_d = 20^\circ$. The simulation cases include: (i) steady-state response, and (ii) source/loading variation. Besides, the hardware circuit of SISCC is realized as photo shown in Fig. 6. There are two parts including: (i) power part of SISCC (right: $14\text{cm}\times10\text{cm}$), (ii) ASN and PWM controller (left: $14\text{cm}\times10\text{cm}$), mainly implemented in the circle-marked chip (I.C. number: D35-101B-37e, TSMC 0.35μm 2P4M, size: 500μm×300μm, 12.2mW, max. frequency: 200kHz) via full-custom fabrication of National Chip Design and Implementation Center (CIC), Taiwan. Fig. 7 shows the physical layout and wire-bonding diagrams of D35-101B-37e. Finally, this hardware circuit is tested practically for the same cases.

Firstly, the simulation is discussed here. (i) Steady-state response: The SISCC is simulated for $V_{\text{ref}} = 80\text{V}, 75\text{V}$ respectively, and the waveforms of $V_o$ and the relevant ripples are shown as in Fig. 8(a)-(d). In Fig. 8(a) and 8(c), it is found that the converter is stable to keep $V_o$ on following $V_{\text{ref}}$, and the settling time is shorter than $20\text{ms}$. In Fig. 8(b) and 8(d), the output ripple percentage can be obtained as: $rp = 0.05\%$. Also, the efficiencies are obtained as: $\eta = 88.9\%, 89.4\%$, and the results can be verified by (10). Additionally, Fig. 8(e) deals with the steady-state waveforms of duty cycle, capacitor voltage, and inductor current for $V_{\text{ref}} = 80\text{V}$. (ii) Source/loading variation: [Case I]: Assume supply source $V_S$ is 5V normally, and it suddenly has a voltage drop from 5V to 4.5V at 60ms. After a short period, $V_S$ recovers from 4.5V to 5V at 90ms. Fig. 8(f) shows the waveform of $V_o$ while $V_S = 5\text{V} \rightarrow 4.5\text{V} \rightarrow 5\text{V}$, and it is found that $V_o$ has a very small drop of 0.05V at 60ms $\sim$ 90ms. Obviously, the closed-loop SISCC still can hold $V_o$ on following $V_{\text{ref}} = 80\text{V}$ in spite of the source variation. [Case II]: Assume $R_L$ is 500Ω normally, and it suddenly changes from 500Ω to 250Ω (double loading) at 60ms. After a short period, $R_L$ changes from 250Ω back to 500Ω at 95ms. Fig. 8(g) shows the waveform of $V_o$ while $R_L = 500\Omega \rightarrow 250\Omega \rightarrow 500\Omega$, and it is found that $V_o$ has a very small drop of 0.02V at 60ms $\sim$ 95ms. Clearly, $V_o$ is still following $V_{\text{ref}} = 60\text{V}$ in spite of the loading variation. The results show that the converter has good robustness to source/loading variation. Here, a remark is given about the switch utilization by using ASN. Fig. 9(a) shows conversion ratio $M_n$ versus duty cycle $D$, and Fig. 9(b) shows switch utilization $P_o/P_T$ versus duty cycle $D$. When $V_o$ (i.e. $V_{\text{ref}}$) is desired at 50V, the step-up gain is $V_{\text{ref}}/V_S = 50/5 = 10$. As the bold line: $n = 0$ shown in Fig. 9(a) (i.e. with no front-stage SC and ASN), $D$ needs a high duty of 0.8 for this gain of 10, and the switch utilization is $P_o/P_T = 20\%$ as in Fig. 9(b). As the dotted line: $n = 1$, $D$ needs 0.6 for this gain and $P_o/P_T = 40\%$. As the star line: $n = 2$, $D$ needs just a smaller duty of 0.4 for this same gain, and the switch utilization can be improved to $P_o/P_T = 60\%$. Thus, based on ASN control, $n \ (n = 0,1,2,\ldots,n_c)$ can be adapted according to $V_S$ and $V_{\text{ref}}$ to obtain a properly small $D$ for the higher switch utilization, i.e. reduce the voltage/current stress on power switch.

Secondly, the experiment is discussed as follows. ($V_S = 5\text{V}, R_L = 5\text{k}\Omega, f_S = 15\text{kHz}$, tool: Agilent 54830B/MS0-X 3052A oscilloscope, probe attenuation: 10x). (i) Steady-state response: The hardware of SISCC is tested for $V_{\text{ref}} = 80\text{V}, 75\text{V}$ respectively, and the waveforms of $V_o$ and the relevant duty cycle are shown as in Fig. 10(a)-(d). In Fig. 10(a) and 10(c), the output signal is measured at 8.019V, 7.505V respectively, i.e. $V_o$ has the steady-state practical value of about 80.19V, 75.05V, and is following $V_{\text{ref}} = 80\text{V}, 75\text{V}$ via the controller. In Fig. 10(b) and 10(d), the duty cycle is measured at 0.633, 0.604 respectively for two different $V_{\text{ref}} = 80\text{V}, 75\text{V}$. Also, the ripples
and efficiencies are measured as \( r_p = 1.25\% , 0.96\% \), \( \eta = 84.3\% , 87.2\% \). (ii) Source/loading variation: [Case I]: Assume \( V_S \) suddenly changes from normal 5V down to 4.5V, and after a short period \( V_S \) recovers from 4.5V to 5V. Fig. 10(e) shows the waveform of \( V_o \) while \( V_S = 5V \to 4.5V \to 5V \). It is found that \( V_o \) has a very small drop, but the closed-loop SISCC still can hold \( V_o \) on following \( V_{ref} = 80V \). [Case II]: The SISCC hardware is tested for loading variation. Fig. 10(f) shows the total waveform of \( V_o \) when the same load is added in parallel and then the added load is removed after about 3.5 sec \( (V_{ref} = 60V) \). Obviously, \( V_o \) has an abrupt drop while the same load is added in, and has an abrupt jump while the added load is removed, but \( V_o \) is still following \( V_{ref} = 60V \) for achieving the output regulation.

6. Conclusions

This paper presents the analysis, design and implementation of a closed-loop ASN-based SISCC for the step-up DC-DC conversion & regulation. The power part of SISCC consists of two cascaded sub-circuits: a serial-parallel SC circuit with \( n_c \) pumping capacitors and a SI booster with \( m_c \) resonant capacitors, so as to obtain a high step-up gain of \( (n_c+1) \times m_c / (1-D) \) at most, where \( D \) is the duty cycle of PWM. Further, the ASN control is presented with adapting the stage number \( n \) \( (n=0,1,2,\ldots,n_c) \) of the front-stage capacitors to realize a flexible gain of \( (n+1) \times m_c / (1-D) \), and then according to \( V_S \) and \( V_{ref} \) so as to obtain a properly small duty cycle \( D \) for improving switch utilization and/or supply voltage range. The control part consists of ASN decision, ASN phase generator and PWM compensator, mainly implemented in the chip via full-custom fabrication (TSMC 0.35μm 2P4M). The advantages of the proposed scheme are listed as follows. (i) As the example said, the step-up gain of 16.2 or higher can be achieved just with one inductor, four switches and five capacitors. Thus, this scheme can provide the high step-up gain under the fewer component count, or under a compromise among volume size, component count, and voltage gain. (ii) For the higher step-up gain required, it can be realized easily by extending the stage number of pumping capacitors. (iii) Since the dominant pole of SISCC is in the left half of s-plane, this scheme has an inherent good local stability. (iv) The ASN control is presented here with adapting the stage number \( n \) \( (n=0,1,2,\ldots,n_c) \) to realize a flexible step-up gain according to \( V_S \) and \( V_{ref} \) so as to obtain a properly small duty cycle \( D \) for improving switch utilization and/or supply voltage range. (v) The PWM technique is adopted here not only to enhance output regulation capability for the different desired outputs, but also to reinforce the output robustness against source/loading variation.

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References

Dickson J. K. On-chip high voltage generation in NMOS integrated circuits using an improved voltage multiplier technique. {

Tanzawa T. and Tanaka T. A dynamic analysis of the Dickson charge pump circuit. {

Mak O. C., Wong Y. C., and Ioinovici A. Step-up DC power supply based on a switched-capacitor circuit. {

Chang H. and Ioinovici A. Switched-capacitor-based DC-to-DC converter with improved input current waveform. {

Palumbo G., Pappalardo D., and Gaibotti M. Increase circ...
Fig. 1. Configuration of ASN-based SISCC.
Fig. 2 Theoretical waveforms of SISCC.
Fig. 3. Topologies of SISCC in (a) Phase I, (b) Phase II, (c) Phase III.
Fig. 4 Equivalent circuits in the period of (a) PWM-ON (b) PWM-OFF.

Fig. 5. Control diagram of ASN-based SISCC.
Fig. 6. Hardware implementation of SISCC.

Fig. 7. D35-101B-37e: (a) Physic layout diagram, (b) Wire-bonding diagram.
Fig. 8. Steady-state response: $V_o$ and $r_p$ for $V_{ref} = (a)(b) 80\, \text{V}, (c)(d) 75\, \text{V};$

(e) Waveforms of $D, S_0, S_1, S_2, I_L, V_{C1},$ and $V_{C2}$ for $V_{ref} = 80\, \text{V}.$

Dynamic response: (f) $V_o$ and $V_S$ for $V_{ref} = 80\, \text{V}$ while $V_S = 5\, \text{V} \rightarrow 4.5\, \text{V} \rightarrow 5\, \text{V}.$

(g) $V_o$ and $V$ for $V_{ref} = 60\, \text{V}$ while $R_L = 500\, \Omega \rightarrow 250\, \Omega \rightarrow 500\, \Omega$ ($V$: the signal of double loading).
Fig. 9. (a) Conversion ratio versus duty cycle for various stage numbers.
(b) Switch utilization versus duty cycle.
(a) $V_o=80.19\text{V}$
   $r_p=1.25\%$

(b) $D=0.633$

(c) $V_o=75.05\text{V}$
   $r_p=0.96\%$
Fig. 10. Steady-state response: $V_o$, $r_p$, and $D$ for $V_{\text{ref}} = (a)(b) 80\,V$, (c)(d) $75\,V$ ; Dynamic response: (e) $V_o$ for $V_{\text{ref}} = 80\,V$ while $V_s = 5\,V \rightarrow 4.5\,V \rightarrow 5\,V$ ; (f) $V_o$ for $V_{\text{ref}} = 60\,V$ while $R_L = 5k\Omega \rightarrow 2.5k\Omega \rightarrow 5k\Omega$ .