Modeling and Analysis of Two-Stage Current-Mode Multiphase Voltage Doubler

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Abstract

A methodology about modeling and analysis of switched-capacitor-based (SC) two-stage current-mode multiphase voltage doubler (MPVD) is suggested for the low-power step-up DC-DC conversion. The SC-based converter needs no magnetic element, so the integrated circuit fabrication will be promising. This current-mode MPVD can obtain the high boosting voltage gain just by using the least number of pumping capacitors, so it will save the device areas more. Besides, with a current source and pulse-width-modulation (PWM) control, a closed-loop current-mode MPVD is proposed not only to enhance regulation capability for different desired outputs, but also to reinforce output robustness against source noises. Here, the system modeling and theoretical analysis are including: state-space averaging model, steady-state DC analysis, transient AC analysis, power conversion efficiency, output ripple percentage, output capacitance selection, and system stability. Finally, the closed-loop current-mode MPVD is simulated by OrCAD, and the results are illustrated to show the efficacy of the proposed scheme.

Keywords: switched-capacitor, current-mode, multiphase voltage doubler, PWM, step-up conversion.
1. Introduction

In general, a charge pump SC converter is designed to obtain an output voltage higher than times the supply voltage or a reverse-polarity voltage. In the last decade, the various types of charge pumps were suggested for power conversion, and the most famous topologies of them are both: Dickson [1-2] and Makowski [3-4]. Dickson charge pump is composed of a diode chain connected with two-phase clock via pumping capacitors. It can provide a step-up voltage gain proportional to the stage number of pumping capacitors [1]. But, it always requires the larger device area to implement VLSI when a larger voltage gain is asked. Makowski charge pump is composed of the two-phase cascaded voltage doublers [3]. By the two-phase clock for charge control, an \( n \)-stage Makowski charge pump can obtain the boosting voltage gain limited by the \( (n+1) \)th Fibonacci number. General speaking, these charge pumps have the larger rise time due to the cascaded scheme. But, on the other hand, they have the advantage of the lower voltage stress for each pumping capacitor than other SC converters do, so it is helpful to pumping capacitor fabrication. In addition, Makowski charge pump has been proved just to require the least number of pumping capacitors in the two-phase SC converters [4]. To follow this idea, Starzyk proposed a new charge pump scheme, called MPVD, and the most different point is to apply multiphase clocks for charge control [5]. By such a multiphase control, it is achieved that the voltage gain increases up to \( 2^n \) at most in the \( n \)-stage MPVD. So, for the same voltage gain, the number of pumping capacitors in Starzyk is required fewer than that in Makowski, i.e., such a MPVD has the lower cost of fabrication area. Nevertheless, some improvement spaces still exist, e.g. regulation capability, and output robustness against source noises. Here, the idea of the current-mode SC converter [6] is adopted for charging capacitors via current source so as to improve the output robustness. Following the same idea, Chang also proposed an integrated scheme of SC step-down/step-up DC-DC converter/DC-AC inverter [7-9]. In this paper, a closed-loop two-stage current-mode MPVD is proposed based on PWM for step-up DC-DC conversion. Based on the current-mode PWM, this MPVD possesses not only regulation capability for different output commands, but also output robustness against source noises/disturbances.

2. Configuration of Two-Stage Current-Mode MPVD

Fig. 1 shows an overall closed-loop two-stage current-mode MPVD with PWM control, and it contains two major parts: “power part” and “control part”. The power part, called a current-mode MPVD step-up converter as shown in the upper half of Fig. 1, is proposed and modified based on two-stage Starzyk charge pump [5]. This modified MPVD is basically composed of two voltage doublers and one current source in series connection between source \( V_S \) and output \( V_o \). For more details, it includes 2 pumping capacitors \( C_1, C_2 \) & 8 switches \( S_{1n}, S_{lp}, \cdots S_{4p} \), where each capacitor has the same capacitance \( C \) (\( C_1 = C_2 = C \)) with equivalent series
resistance (ESR) \( r_C \), and similarly the output capacitor has capacitance \( C_o \) with ESR \( r_{C_o} \), and \( S_{1n} \), \( S_{1p} \), \( \cdots \), \( S_{4p} \) are operated as static switches with the on-state resistance \( r_T \). The basic operation of the modified MPVD is as follows. In addition, for the current-mode operation, one constant current source \( I_D \) is added here, and realized by using one current reference and two current mirrors. First, the bias current reference \( I_m \) is set and adjusted by resistor \( R_m \). And then, the two current mirrors carry out the current copiers with the ratios of \( a_1 \) and \( a_2 \). With the help of current reference and current mirrors, the current source \( I_D \) can be realized and assigned to the value of \( a_1a_2 \cdot I_m \).

Next, let’s look at the basic operation of the current-mode MPVD. Fig. 2 shows the theoretical waveforms of this MPVD. Here, one switching cycle \( T_S \) is divided into four phases (Phase I-IV) with the same quad-cycle value of \( T \) \((T_S = 4T)\). In the first quad-cycle (Phase I), let \( S_1 \) turn on (including PMOS \( S_{1p} \) and NMOS \( S_{1n} \)), and then voltage \( v_{C1} \) across \( C_1 \) is charged up to \( V_S \). In the second quad-cycle (Phase II), let \( S_2 \) and \( S_3 \) turn on, and voltage \( v_{C2} \) across \( C_2 \) is charged by the series connection with \( V_S \) and \( v_{C1} \). In the third quad-cycle (Phase III), it repeats the Phase I operation. In the forth quad-cycle (Phase IV), let \( S_2 \) and \( S_4 \) turn on, and under the series connection with \( V_S \), \( v_{C1} \), and \( v_{C2} \), voltage \( v_{C0} \) across \( C_o \) is charged via the constant current source \( I_D \) in the time interval of \( t \in [t_3, t_3 + DT] \) to supply the load \( R_L \). Based on the scheduled operation cyclically, output voltage \( v_o \) can be regulated relative to how long the charging time \( DT \) is. Because of the two-stage scheme employed here, the step-up function can be realized so that the maximum output \( v_o \) can be boosted up to 4 times voltage of source \( V_S \) ideally.

Secondly, the control part: PWM controller is used here as shown in the lower half of Fig. 1, and it is functionally composed of low-pass filter (LPF), PWM block and phase generator. First, from the view of controller signal flow, the feedback output current \( i_o \) is sent into LPF for high-frequency noise rejection. Next, the filtered signal \( I_o \) is compared with the desired output reference \( I_{ref} \) so as to produce the duty
Fig. 1 Configuration of two-stage current-mode MPVD

Fig. 2 Theoretical waveforms of current-mode MPVD
cycle $D$ via the PWM block. At the same time, a phase signal generator can be realized based on frequency divider to generate the MOSFET drive signals $S_1 - S_4$ according to Fig. 2. Here, to realize duty cycle control in Phase IV, signal $S_{4n}^*$ in Fig. 1 can be generated via logic AND combination between signal $S_{4n}$ and duty cycle $D$. In this paper, by using the current-mode PWM control, the regulation capability of MPVD will be improved for different desired outputs.

### 3. Modeling of Two-stage Current-Mode MPVD

In this section, let’s move on the modeling of the current-mode MPVD. According to the four-phase operations in Fig. 2, the formulation of two-stage current-mode MPVD will be derived. Firstly, in Phase I ($t \in [t_0, t_1]$), let $S_1$ turn on and the other MOSFETs be off, and its topology is obtained as shown in Fig. 3(a): $v_{C_1}$ across $C_1$ is charged up to $V_S$. So, the dynamic equation for Phase I can be described as

\[
\begin{bmatrix}
    v_{C_1}'(t) \\
    v_{C_2}(t) \\
    v_{C_0}'(t)
\end{bmatrix} = \begin{bmatrix}
    \frac{-1}{RC} & 0 & 0 \\
    0 & \frac{-1}{RC} & 0 \\
    0 & 0 & \frac{1}{RC} \\
\end{bmatrix} \begin{bmatrix}
    v_{C_1}(t) \\
    v_{C_2}(t) \\
    v_{C_0}(t)
\end{bmatrix} + \begin{bmatrix}
    0 & 0 & I_D \\
    0 & 0 & \frac{1}{V_S} \\
\end{bmatrix}
\]

\[ (1a) \]

\[
\begin{bmatrix}
    v_0(t) \\
    i_S(t)
\end{bmatrix} = \begin{bmatrix}
    0 & 0 & 1 \\
    \frac{-1}{R} & 0 & 0 \\
\end{bmatrix} \begin{bmatrix}
    v_{C_1}(t) \\
    v_{C_2}(t) \\
    v_{C_0}(t)
\end{bmatrix} + \begin{bmatrix}
    0 & 0 & I_D \\
    0 & \frac{1}{V_S} & \frac{1}{V_S} \\
\end{bmatrix}
\]

\[ (1b) \]

where the parasitic resistor $R$ is defined as: $R = 2 \cdot r_T + r_C$, and $v_0(t)$, $i_S(t)$ represent the output voltage and the current at supply terminal, respectively. In addition, the constant current source $I_D$ is treated as an input here, and it can be realized by one bias current reference $I_m$ and two current mirrors with the ratio values of $a_1$ and $a_2$. And then, $I_D$ can be set and assigned to the value of $a_1a_2 \cdot I_m$.

Secondly, in Phase II ($t \in [t_1, t_2]$), let $S_2$ and $S_3$ turn on, and its topology is shown in Fig. 3(b): $v_{C_2}$ across $C_2$ is charged by the series connection with $V_S$ and $v_{C_1}$. So, the dynamic equation for Phase II is derived as

\[
\begin{bmatrix}
    v_{C_1}'(t) \\
    v_{C_2}'(t) \\
    v_{C_0}'(t)
\end{bmatrix} = \begin{bmatrix}
    \frac{1}{2RC} & \frac{1}{2RC} & 0 \\
    \frac{1}{2RC} & \frac{-1}{2RC} & 0 \\
    0 & 0 & \frac{-1}{RC} \\
\end{bmatrix} \begin{bmatrix}
    v_{C_1}(t) \\
    v_{C_2}(t) \\
    v_{C_0}(t)
\end{bmatrix} + \begin{bmatrix}
    0 & 0 & I_D \\
    0 & \frac{1}{2RC} & \frac{1}{2RC} \\
\end{bmatrix}
\]

\[ (2a) \]
\[
\begin{bmatrix}
v_0(t) \\
i_S(t)
\end{bmatrix} = \begin{bmatrix}
0 & 0 & 1 \\
1 & 0 & 0 \\
0 & 0 & 1
\end{bmatrix} \begin{bmatrix}
V_{C1}(t) \\
V_{C2}(t) \\
V_{C_o}(t)
\end{bmatrix} + \begin{bmatrix}
0 \\
0 \\
0
\end{bmatrix} I_D \\
+ \begin{bmatrix}
V_S
\end{bmatrix}
\] (2b)

Thirdly, in Phase III \((t \in [t_2,t_3])\), let \(S_1\) turn on, and its topology is shown in Fig.3(c). Obviously, due to the same topologies in Phase I and III, the dynamic equation for Phase III is completely identical to (1). Finally, in Phase IV \((t \in [t_3,t_4])\), let \(S_2\) and \(S_4\) turn on, and the topology is shown in Fig. 3(d). In this figure, by the series connection with \(V_S\), \(v_{C1}\), and \(v_{C2}\), voltage \(v_{C_o}\) across the capacitor \(C_o\) is charged via the constant current source \(I_D\) in the time interval of \(t \in [t_3,t_3 + DT]\). So, the dynamic

Fig. 3 Multiphase operational topologies
equation for Phase IV is derived as

\[
\begin{bmatrix}
-v_{C_1}'(t) \\
v_{C_2}'(t) \\
v_{C_o}'(t)
\end{bmatrix}
=
\begin{bmatrix}
0 & 0 & 0 \\
0 & 0 & 0 \\
0 & 0 & -\frac{1}{R_L C_o}
\end{bmatrix}
\begin{bmatrix}
v_{C_1}(t) \\
v_{C_2}(t) \\
v_{C_o}(t)
\end{bmatrix}
+ \begin{bmatrix}
-D \\
-D \\
-D
\end{bmatrix}
\begin{bmatrix}
0 \\
0 \\
0
\end{bmatrix}
\begin{bmatrix}
I_D \\
V_S
\end{bmatrix}
\]  

\(3a\)

\[
\begin{bmatrix}
v_o(t) \\
i_S(t)
\end{bmatrix}
=
\begin{bmatrix}
0 & 0 & 1 \\
0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
v_{C_1}(t) \\
v_{C_2}(t) \\
v_{C_o}(t)
\end{bmatrix}
+ \begin{bmatrix}
0 & 0 \\
D & 0
\end{bmatrix}
\begin{bmatrix}
I_D \\
V_S
\end{bmatrix}
\]  

\(3b\)

Based on (1)-(3), let’s take the four-phase average, i.e., \([(1)+(2)+(1)+(3)]/4\), and then the state-space averaged modeling of two-stage current-mode MPVD is formulated as

\[
x'(t) = A_{av} \cdot x(t) + B_{av} \cdot u(t) \]  

\(4a\)

\[
y(t) = C_{av} \cdot x(t) + D_{av} \cdot u(t), \]  

\(4b\)

Where

\[
x(t) = \begin{bmatrix} v_{C_1}(t) & v_{C_2}(t) & v_{C_o}(t) \end{bmatrix}^T, \]  

\(5a\)

\[
u(t) = \begin{bmatrix} I_D & V_S \end{bmatrix}^T \]  

\(5b\)

\[
y(t) = \begin{bmatrix} v_o(t) & i_S(t) \end{bmatrix}^T \]  

\(5c\)

\[
A_{av} = \begin{bmatrix}
-\frac{5}{8RC} & -\frac{1}{8RC} & 0 \\
\frac{1}{8RC} & -\frac{1}{8RC} & 0 \\
0 & 0 & -\frac{1}{R_L C_o}
\end{bmatrix}, \quad B_{av} = \begin{bmatrix}
\frac{D}{4C} & \frac{3}{8RC} \\
\frac{D}{4C} & \frac{1}{8RC} \\
\frac{D}{4C} & 0
\end{bmatrix} \]  

\(5d,e\)

\[
C_{av} = \begin{bmatrix}
0 & 0 & 1 \\
0 & \frac{3}{8R} & \frac{1}{8R} \\
-\frac{1}{8R} & 0 & 0
\end{bmatrix}, \quad D_{av} = \begin{bmatrix}
0 & 0 \\
0 & \frac{D}{4} \\
0 & \frac{5}{8R}
\end{bmatrix} \]  

\(5f,g\)

Here, it is noteworthy that the averaged current-mode MPVD formulation of (4) will be very helpful to the theoretical analysis and control design later.
4. Analysis of Two-Stage Current-Mode MPVD

4.1 Steady-state and transient analysis:

Here, both steady-state and transient analysis of current-mode MPVD will be discussed. First, let’s look at the steady-state analysis. Based on the averaged MPVD formulation of (4), the transfer functions related to $v_o$ and $i_S$ can be derived as

$$v_o(s) = [C_{av,1} \cdot (sI - A_{av})^{-1} \cdot B_{av} + D_{av,1}] \cdot u = \frac{D}{s + \frac{1}{RC}} \cdot I_D$$

$$i_S(s) = [C_{av,2} \cdot (sI - A_{av})^{-1} \cdot B_{av} + D_{av,2}] \cdot u$$

where $C_{av,1}$ and $C_{av,2}$ ($D_{av,1}$ and $D_{av,2}$) are the matrices which are composed of the first and second row of $C_{av}$ ($D_{av}$), respectively. Then, by substituting $s = 0$ of (6), the steady-state output voltage $V_o$, output current $I_o$, and supply-terminal current $I_S$ can be derived as

- Steady-state analysis and expression:
  $$V_o = \frac{D \cdot R_L}{4} \cdot I_D$$  \hspace{1cm} (7a)
  $$I_o = \frac{V_o}{R_L} = \frac{D}{4} \cdot I_D$$  \hspace{1cm} (7b)
  $$I_S = D \cdot I_D$$  \hspace{1cm} (7c)

  From (7b), it is observed that output current $I_o$ is not a function of source $V_S$ and load $R_L$. In other words, when $V_S$ is decreasing or $R_L$ is varying, such a source/load variation does not affect $I_o$ immediately. Truly, by reason of a current source $I_D$ employed here, the source/load variation makes no immediate response on output current $I_o$. This is an excellent advantage of current-mode MPVD for the better output robustness against source/load variations.

Next, let’s look at the transient analysis. First, all variables are divided into two parts as:

$$v_{C_1}(t) = V_{C_1} + \hat{v}_{C_1}(t), \quad v_{C_2}(t) = V_{C_2} + \hat{v}_{C_1}(t), \quad v_{C_o}(t) = V_{C_o} + \hat{v}_{C_o}(t),$$
\[ v_o(t) = V_o + \hat{v}_o(t), \quad i_S(t) = I_S + \hat{i}_S(t), \quad D(t) = D + \hat{d}(t), \]

where \( V_{C_1}, V_{C_2}, V_{C_o}, V_o, I_S, D \) are static operating signals, and \( \hat{v}_{C_1}, \hat{v}_{C_2}, \hat{v}_{C_o}, \hat{v}_o, \hat{i}_S, \hat{d} \) are dynamic small signals. By using the small-signal technique around some static operating point, a dynamic small-signal equation can be derived as shown in (8), and consequently the transfer functions of current-mode MPVD can be also suggested in (9).

- **Small-signal state-space expression:**
  \[
  \begin{bmatrix}
  \hat{\hat{v}}_{C_1}(t) \\
  \hat{\hat{v}}_{C_2}(t) \\
  \hat{\hat{v}}_{C_o}(t)
  \end{bmatrix} = \begin{bmatrix}
  -5/R_{C_1} & -1/R_{C_2} & 0 \\
  1/R_{C_1} & -1/R_{C_2} & 0 \\
  0 & 0 & -1/R_{L}C_o
  \end{bmatrix} \begin{bmatrix}
  \hat{v}_{C_1}(t) \\
  \hat{v}_{C_2}(t) \\
  \hat{v}_{C_o}(t)
  \end{bmatrix} + \begin{bmatrix}
  -I_D/4C_o \\
  I_D/4C_o \\
  I_D/4C_o
  \end{bmatrix} \cdot \hat{d}(t),
  \]
  \( (8a) \)

  \[
  \begin{bmatrix}
  \hat{\hat{v}}_o(t) \\
  \hat{\hat{i}}_S(t)
  \end{bmatrix} = \begin{bmatrix}
  0 & 0 & 1 \\
  -3/R & -1/R & 0
  \end{bmatrix} \begin{bmatrix}
  v_{C_1}(t) \\
  v_{C_2}(t) \\
  v_{C_o}(t)
  \end{bmatrix} + \begin{bmatrix}
  0 \\
  I_D/4
  \end{bmatrix} \cdot \hat{d}(t).
  \]
  \( (8b) \)

- **Small-signal transfer function expression:**
  \[
  G_1(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{I_D}{4C_o} \cdot \frac{s + 1/R_{L}C_o}{s},
  \]
  \( (9a) \)

  \[
  G_2(s) = \frac{\hat{i}_S(s)}{\hat{d}(s)} = \frac{I_D}{s^2 + 3/4RC} \cdot \frac{s + 1/16RC^2}{s + 1/8RC} + \frac{I_D}{4}.
  \]
  \( (9b) \)

If the current-mode MPVD is regarded as an open-loop system, then the open-loop model has been derived as (7)–(9) for control design later. Certainly, some compensation techniques can be applied, for example, output feedback PWM control to form a closed-loop MPVD for the better performances.

### 4.2 Power conversion efficiency:

Based on steady-state analysis of (7), its steady-state input/output power can be computed as:

\[
P_i = V_S \cdot I_S = V_S \cdot D \cdot I_D,
\]
\( (10a) \)
Thus, by combining (10a) and (10b), the power conversion efficiency is derived as

\[
\eta = \frac{P_o}{P_i} = \frac{V_o \cdot \frac{D}{4} \cdot I_D}{V_S \cdot D \cdot I_D} = \frac{1}{4} \cdot \frac{V_o}{V_S} = \frac{M}{4},
\]

(11a)

\[
M = \frac{V_o}{V_S} = \frac{R_L \cdot I_D}{4V_S} \cdot D.
\]

(11b)

where \( M \) represents the DC-DC step-up voltage conversion ratio, and it can be regulated by duty cycle \( D \). From (11a), it is observed that efficiency \( \eta \) is increasing with adding conversion ratio \( M \). In fact, \( \eta \) is not larger than 100% absolutely, so \( M \) must be smaller than 4 for two-stage scheme, i.e., \( V_o \) is boosted up to 4 times the voltage of \( V_S \) at most. For nominal conditions, the maximum attainable output \( V_o \) is \( 4V_S \) – voltage drops in the charging and discharging circuits. But, when \( M \) is operating at the value much smaller than 4 (\( V_o << 4V_S \)), the efficiency will be quite bad. For the better efficiency, it is good to choose the desired output \( V_o \) near \( 4V_S \) as close as possible. If it is not realized, ones can also fit \( 2^n \cdot V_S \) for the desired \( V_o \) by changing the stage number \( n \) and source \( V_S \) for the better efficiency.

4.3 Output ripple and capacitance selection:

According to Fig. 2, output voltage \( u_o \) across \( R_L \) is decaying exponentially from \( V_{o,max} \) to \( V_{o,min} \) during the discharging time interval of \((4 - D)T\) cyclically, and then it can be modeled as:

\[
v_o(t) = V_{o,max} \cdot e^{-t/\tau}, \quad 0 \leq t \leq (4 - D)T
\]

(12)

where \( T = T_S/4 \), and \( T_S \) is the MPVD switching cycle. In the discharging interval, the maximum/ minimum output is \( V_{o,max} / V_{o,min} \), where \( V_{o,max} = v_o(0), V_{o,min} = v_o((4 - D)T) = V_{o,max} \cdot e^{-(4-D)T/\tau} \), and the discharging time constant \( \tau = R_L \cdot C_o \). So, the output ripple variation can be defined as:

\[
\Delta V_o = V_{o,max} - V_{o,min} = V_{o,max} \cdot [1 - e^{-(4-D)T/\tau}].
\]

(13)

Then, the averaged output voltage can be calculated by (12) as:

\[
V_o = \frac{1}{(4 - D)T} \int_0^{(4 - D)T} v_o(t) \, dt = \frac{4}{4 - D} \cdot f_S \cdot \tau \cdot \Delta V_o.
\]

(14)

By combining (13) and (14), the output ripple percentage can be presented as:
Here, it is found that the ripple percentage \(rp\) is worse while the load is being heavier, but it can be improved by increasing switching frequency \(f_s\) or output capacitor \(C_o\). Obviously, when the MPVD is unloaded \((R_L \to \infty)\), \(rp\) is almost zero. For a desired ripple percentage \(\bar{rp}\) and a specified switching frequency \(f_s\), based on (15) plus the heavy load consideration as \(D=1\), the minimum output capacitor can be estimated as

\[
C_o \geq C_{o, \text{min}} = \frac{3}{4 \cdot f_s \cdot R_L \cdot \bar{rp}}.
\] (16)

4.4 Stability of current-mode MPVD:

Let’s look at the stability of the open-loop current-mode MPVD. According to the MPVD formulation of (4), the system characteristic equation and its roots can be computed as:

\[
\Delta(s) = \left| sI - A_{av} \right| = \left( s + \frac{1}{R_L C_o} \right) \left( s^2 + \frac{3}{4RC} s + \frac{1}{16R^2C^2} \right) = 0,
\] (17a)

\[
p_1 = -\frac{1}{R_L C_o}, \quad p_2 = -\frac{3 - \sqrt{5}}{8RC}, \quad p_3 = -\frac{3 + \sqrt{5}}{8RC}.
\] (17b,c,d)

For the better conversion performances, the value of load resistance \(R_L\) is supposed to be much larger than value of parasitic \(r_T, r_C\). In fact, the value of load \(R_L\) is about in \(\Omega\) -level, and the parasitic \(r_T, r_C\) is about in \(m\Omega\) -level \((R_L >> r_T, r_C)\). Besides, according to (16), the value of output capacitor \(C_o\) would be chosen larger for the better output ripple, even times greater than the value of pumping capacitor \(C\) in general. So, the value of \(R_L C_o\) is much larger than the value of \(8RC\) \((R_L C_o >> 8RC)\). Consequently, \(p_1\) dominates the MPVD stability, and \(p_1\) is called the open-loop system’s dominant pole as shown in (17b). Obviously, this open-loop current-mode MPVD is locally stable because this dominant pole \(p_1\) is located in the left half of s-plane. Furthermore, the dominant pole \(p_1\) is not a function of static operating points, so it almost ensures the global stability of the current-mode MPVD. Thus, it is one of advantages that MPVD scheme has an inherent good stability.
5. Example of Two-Stage Current-Mode MPVD

In this section, a closed-loop two-stage current-mode MPVD with PWM control is made in circuit layout and simulated by OrCAD tool, and then the results are illustrated to verify the efficacy of the proposed MPVD scheme. This MPVD is assumed preparing to supply a WLED bank composed of 3 WLEDs in series connection. Here, assume that the normal running voltage/current for each WLED is 3.3V/33mA, so the nominal resistance of each WLED is about 100Ω. Thus, the total resistance of this bank is about 300Ω (RL = 300Ω). By such a series connection, it is sure to keep the running current identical so as to balance the brightness of each WLED. The brightness balance is very important for the back-light application. But, on the other hand, due to such a series scheme, this bank always needs the load voltage higher than the supply voltage, so a step-up converter is necessary. Here, according to Fig 1, the current source ID is chosen with the value of 180mA, and then the two-stage current-mode MPVD converter is realized and employed for the boosting function of 4 times the supply voltage VS at most.

(i) Firstly, this MPVD is operated at the switching frequency of 20kHz to boost the output V0 being at most 4 times the source VS of 3.6V for supplying the WLED bank load RL of 300Ω. Here, for the desired Iref of 40mA, the output current and the steady-state output voltage ripple are simulated, and their results are shown in Fig. 4. In Fig. 4(a), it is obvious that the MPVD converter has a stable work on output conversion for the desired current, and the steady-state output current IO are conclusively about 40mA after the setting time of about 30ms. The output current IO is sure to follow Iref via the current-mode PWM. In Fig. 4(b), the relative output ripple percentage is measured as: rp = ΔV0/V0 = 0.237%, and the power efficiency is obtained as: η = 81.4%. These results show that the current-mode MPVD converter has a pretty good output conversion and steady-state performance.

(ii) Secondly, let’s look at the output robustness to source noises. Since the source voltage is decreasing naturally with the running time of battery, or varying due to the bad quality battery, the output robustness against source noises must be considered. In the first case, it is assumed that source VS starts at DC 3.6V, and then to have a exponential decrease at 25ms from 3.6V to 3.0V, as shown in the upper half of Fig. 5. For the desired Iref of 33mA, the output current is simulated as shown in the lower half of Fig. 5. Obviously, the steady-state IO is still firmly following the desired Iref of 33mA, even though VS has an exponential drop to the voltage lower than standard source of 3.6V. In the second case, for the same desired Iref, VS is assumed to have the DC value of 3.6V and extra sinusoidal disturbance with peak 0.2V, as shown in the upper half of Fig. 6. Then, the output current is obtained as shown in the lower half of Fig. 6. Obviously, IO is sure to follow Iref of 33mA in spite of the supply source with sinusoidal disturbance. So, these results show that the current-mode MPVD has the good output robustness to
source variation or noise.

Fig. 4(a) Output current ($I_{\text{ref}} = 40\text{mA}$)

Fig. 4(b) Output voltage ripple ($I_{\text{ref}} = 40\text{mA}$)

Fig. 5 Output robustness to source decaying ($I_{\text{ref}} = 33\text{mA}$)
6. Conclusion

A closed-loop SC scheme of two-stage current-mode MPVD is proposed based on PWM control to achieve low-power step-up DC-DC conversion and output current regulation. In this paper, by combining a constant current source and PWM control, a closed-loop current-mode MPVD is suggested not only to enhance the regulation capability for the different output commands, but also to reinforce output robustness against the source disturbances. In addition, some relevant theoretical analysis and design are discussed. Finally, a closed-loop two-stage current-mode MPVD is designed by PSPICE, and the results are illustrated to show the efficacy of the proposed MPVD scheme. The advantages of the proposed scheme are involved as follows. (i) The SC-based MPVD scheme needs no magnetic element, so I.C. fabrication will be promising. (ii) This MPVD can obtain the high voltage gain just by using the least number of pumping capacitors, so it will save the device areas more. (iii) Since the current-mode scheme is employed here, the steady-state outputs $V_o$ and $I_o$ are not a function of $V_S$ as shown in (7), so source variation will not make immediate response on the output. Therefore, the current-mode MPVD has the good output robustness against source noises/disturbances. (iv) According to stability analysis, the dominant pole is located in the left half of s-plane, so the open-loop MPVD converter is locally stable. Thus, the MPVD scheme has an inherent good stability.
References


二階電流模式多相式倍壓器之建模與分析

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摘 要

本文提出一個有關於「以切換式電容為主之二階電流模式多相式倍壓器之建模及分析」的方法論，已達成低功率升壓轉換的目的。事實上，SC 電路並不需
要任何電感性元件，因此極有助於未來積體電路的設計與製程實現。此一電流模
式多相式倍壓器能以最少的升壓電容數目，來達成高升壓倍率的要求，因此它能
省掉許多元件。此外，結合使用一電流源與脈波寬度調變技術所形成之閉路的電流模式多相式倍壓器，不僅能增強系統對不同輸出要求之調整能力，亦可提
升對電源雜訊干擾的強健能力。本文中所提出的系統建模及理論分析包含有：狀
態空間平均模式、穩態直流分析、暫態交流分析、功率轉換效率、輸出漣波百分
比、輸出電容選定、以及系統穩定度。最後，本文利用 OrCAD 環境來進行電路
系統的模擬，其各項模擬結果可以驗證所提方法架構之有效性。

關鍵詞：切換式電容，電流模式，多相式倍壓器，脈波寬度調變，升壓轉換。