ABSTRACT

A simple quasi-switched-capacitor (QSC) step-down DC-DC converter with multiple output choice (9V/5V, 9V/3.3V, 9V/2V) is designed and implemented via complex-programmable-logic-device-based (CPLD) digital controller for low-power applications (Input: 7.0–9.0V, load: 50–400Ohms). The integrated digital controller is implemented by combination with Verilog CPLD and ADC/DAC chips to achieve the closed-loop control of QSC converter. Such a Verilog-based CPLD can make controller design more flexible, simple and reliable. In fact, SC circuit needs no inductive element, so I.C. fabrication is promising, and it is pretty suitable for low-power VLSI applications. An interleaved current-mode control is employed here from battery source interleaved charging to the series capacitors of different cells by a voltage-controlled current source, so the continuous input current comes into being, and it results in a good feature: low electromagnetic interference (EMI). Such a current-mode control is able to not only enhance output robustness against source variation/noise, but also keep regulation capability of converter with loading variation. Finally, the hardware experiments are illustrated to show the efficacy of the scheme designed, including voltage conversion and output ripple, and output robustness against source variation.

Keywords: quasi-switched-capacitor, step-down, DC-DC converter, Verilog-code, CPLD.
1. Introduction

In recent years, due to the popularity of potable electronic equipments, for example, PDA, notebook, cellular phone, digital camera, pager, and e-book …etc., their DC-DC power module always asks for some good features of small volume, light weight, high power density and efficiency, and good regulation capability. Besides, to fit in with requirements of various functions all in one, both multiple output choice and flexible controller design become essential to power module design gradually. Therefore, more manufactures and researchers pay much attention to this topic on development of a more flexible power converter for low-power applications, ultimately requiring DC-DC converters realized on a chip by mixed analog VLSI technology. In 1996, Chung and Ioinovici suggested a completely new converter scheme, called quasi-switched-capacitor (QSC) step-down converter, employed by current-mode control idea [1]. Basically, this converter configuration is composed of two SC cells working in anti-phase periods. In fact, this configuration is almost similar to that of Cheong’s [2], but the most different point between them is to use a constant current source for charging capacitors (current-mode), not to use a constant voltage source (voltage-mode). Here, some MOSFETS are operated in pinch-off region as a voltage-controlled current source, so the capacitor voltage is linearly changed with time, not exponentially charged as [2]. Thus, the input current is continuous and constant, but not discontinuous and variant as [2], so EMI problem can be improved. From 1999, researchers are concentrated mainly in regulation improvement and capability enhancement of the QSC converter [3]-[8]. Henry suggested a multi-stage design of QSC DC-DC converter for improving voltage regulation and current drive capability [3]. For step-down design, $n$ capacitors are discharged in parallel, and then the larger output current can be generated for the heavier load drive [4]. For step-up design, $n$ capacitors are discharged in series for supplying the higher voltage load [5]. However, some improvement spaces still exist, for example, multiple output choice, controller reliability, and controller design flexibility. In this paper, based on the CPLD-based digital controller, a simple QSC step-down DC-DC converter with multiple output choice is implemented for a variety of low-power output. Such a Verilog-code-based CPLD chip can make controller design more flexible, simple, and reliable.
2. Configuration of CPLD-Based Converter

2.1 CPLD-Based QSC Converter Scheme

Fig.1 shows the overall circuit configuration of CPLD-based QSC step-down DC-DC converter, and it contains two parts: “power part” and “control part” for achieving the closed-loop control of QSC converter with multiple output choice. First, the above half of Fig.1 deals with the power part: QSC step-down DC-DC converter, which is composed of capacitors and MOSFETS [1]. The basic control operation is described as follows. In the first half-cycle, let $Q_{SA}$ operate in pinch-off region as a constant controlled current source, turn off $S_A$ and $Q_{SB}$, and turn on $S_B$ in triode region as a small resistor. Thus, all capacitors of cell A are linearly charged by the constant current source. At the same time, all capacitors of cell B are discharged to supply the load $R_L$. Based on the same idea, in the second half-cycle, exchange the works of two cells, and then run the operation cyclically. Thus, it is obvious that the output $v_o$ can be regulated relative to how much the capacitors are charged by controlled current source. Fig.2 shows the theoretical current waveforms of this QSC converter. Secondly, the control part: CPLD-based digital controller is shown in Fig.1 below, which is composed of Verilog-code-based CPLD, ADC/DAC chips, crystal oscillator, and low-pass filter. From the view of controller signal flow, the feedback signal of the converter: output $v_o$ is sent into the OP-amp low-pass filter for high-frequency noise rejection, and next the filtered signal is transferred into the digital form by an ADC chip. Then, the filtered/digitalized output is sent into the CPLD chip, and then compared with the desired output reference (selected by the multiple output choice) to produce the digital-form control signal $v_{GS}$. Next, with the DAC chips, this digital-form control signal $v_{GS}$ is transferred back into the analog form, and then to adjust the drain current $i_D$ ($I_{QSA}/I_{QSB}$ of $Q_{SA}/Q_{SB}$) for the capacitor voltage regulation of two cells. So, the Verilog-based CPLD has two tasks to do: (i). dynamic production of the digital control signal $v_{GS}$ according to both the filtered/digitalized output and the desired output reference, and (ii). static generation of the timing-control signals of QSC cells according to the scheduled operation of Fig.2. Here, by using Verilog programming, the CPLD-based digital controller has a more flexible, simple and reliable design process for multiple output choice.

2.2 Formulation of QSC Step-Down Converter

By increasing the number of capacitors of two cells in the above half of Fig.1,
a circuit configuration of n-stage QSC step-down DC-DC converter is suggested and extended here. This n-stage QSC converter is still composed of two n-stage cells A and B in parallel between source $V_S$ and output $V_O$. For each cell, there includes $n$ capacitors $C_1, C_2 \cdots C_n$, and $3n-1$ MOSFET switches $S_1, S_2 \cdots S_{3n-1}$, where each capacitor has capacitance $C$ with equivalent series resistance (ESR) $r_C$, and similarly the output capacitor has capacitance $C_o$ with ESR $r_{Co}$, and MOSFETS $S_1, S_2 \cdots S_{3n-1}$ are operated as static switches with the on-state resistance $r_T$. According to the scheduled operation of Fig.2, it is obvious that both cells A and B are basically operated in anti-phase: when cell A is in the capacitor-charging period, cell B is working in the capacitor-discharging period, and vice versa. So, the duty cycle is fixed at 0.5 for each cell. Here, in the first half-cycle period, let $Q_{SA}$ be in pinch-off region as a controlled current source, turn off $S_A$ and $Q_{SB}$, and turn on $S_B$ in triode region as a small resistor. Then, $n$ capacitors $C_{A1} \sim C_{An}$ of cell A are linearly charged in series by the constant...
controlled current source, and at the same time, n capacitors $C_{B1} \sim C_{Bn}$ of cell B are discharged in parallel to supply the load $R_L$. Based on the same idea, in the second half-cycle, they exchange their works. By this way, charging in series and discharging in parallel for n capacitors cyclically, the step-down function can be realized to keep output on $V_S/n$ ideally. Here, for simplification, since all capacitors of cells A and B are selected identically by the value of $C$, in other words, that is $C_{A1} = \cdots = C_{An} = C_{B1} = \cdots = C_{Bn} = C$, the voltage drop across each capacitor of the same cell is assumed identical, denoted by $v_{Ca}(t)$ and $v_{Cb}(t)$ for capacitor voltage in cells A and B, respectively. According to these two circuit topologies (charging into n capacitors in series and discharging from n capacitors in parallel), a complete state-space averaged description of n-stage QSC step-down DC-DC converter can be derived as
Fig. 2 Theoretical current waveform
\[
\begin{bmatrix}
V_{Ca}(t) \\
V_{Cb}(t) \\
V_{Co}(t)
\end{bmatrix} = \begin{bmatrix}
\frac{-r_{Co} + R_l}{2nC \cdot \Delta} & 0 & \frac{R_l}{2nC \cdot \Delta} \\
0 & \frac{-r_{Co} + R_l}{2nC \cdot \Delta} & \frac{R_l}{2nC \cdot \Delta} \\
\frac{R_l}{2C_o \cdot \Delta} & \frac{R_l}{2C_o \cdot \Delta} & \frac{-\eta + r_T + R_l}{C_o \cdot \Delta}
\end{bmatrix}
\begin{bmatrix}
V_{Ca}(t) \\
V_{Cb}(t) \\
V_{Co}(t)
\end{bmatrix} + \begin{bmatrix}
1 \\
\frac{1}{2C} \\
0
\end{bmatrix} \cdot [i_D(t)],
\]
(1a)

\[
\begin{bmatrix}
\Delta \\
\Delta \\
\Delta
\end{bmatrix} = \begin{bmatrix}
\frac{r_{Co} R_L}{2\Delta} & \frac{r_{Co} R_L}{2\Delta} & \frac{(\eta + r_T) \cdot R_L}{\Delta}
\end{bmatrix}
\begin{bmatrix}
\dot{V}_{Ca}(t) \\
\dot{V}_{Cb}(t) \\
\dot{V}_{Co}(t)
\end{bmatrix},
\]
(1b)

where
\[
\eta = (r_C + 2r_T)/n, \quad \Delta = (r_T + \eta)(r_{Co} + R_L) + r_{Co} R_L,
\]
(1c,d)

\[
i_D(t) \text{ is the average drain current of } Q_{SA}/Q_{SB}, \text{ and } V_O(t), V_{Co}(t) \text{ represent the load voltage and output capacitor voltage, respectively.}
\]

In this research, such a QSC configuration is adopted with increasing some advantages as follows. (i) Since the interleaved current-mode technique is adopted, the input current \(I_S\) can be constant continuously. The input current waveform has no high current peak/jump, so that EMI problem is improved greatly. (ii) Since all the elements in power-part circuit contain only MOSFETS and capacitors, the uniform feature is helpful to I.C. fabrication and realization. (iii) Since the two cells are working complementarily, i.e., the duty cycle is fixed at 0.5, such a constant duty cycle is much useful especially to control design and theoretical analysis.

First, for the aim to steady-state analysis, based on the (1), around one static operating point, all voltages and currents are divided into two parts: static operating points and dynamic small signals as:

\[
V_{Ca}(t) = V_{Ca} + \hat{V}_{Ca}(t), \quad V_{Cb}(t) = V_{Cb} + \hat{V}_{Cb}(t), \quad V_{Co}(t) = V_{Co} + \hat{V}_{Co}(t),
\]
(2a,b,c)

\[
i_D(t) = I_D + \hat{i}_d(t), \quad V_O(t) = V_o + \hat{V}_o(t), \quad V_{GS}(t) = V_{GS} + \hat{V}_{gs}(t),
\]
(2d,e,f)

where \(V_{Ca}, V_{Cb}, V_{Co}, I_D, V_o, V_{GS}\) represent the static signals, and \(\hat{V}_{Ca}, \hat{V}_{Cb}, \hat{V}_{Co}, \hat{i}_d, \hat{V}_o, \hat{V}_{gs}\) are the dynamic small signals. By substituting \(x'(t) = 0\) of (1), steady-state output \(V_o\) and \(I_o\) can be shown as

\[
V_o = -C_{av} A_{av}^{-1} B_{av} \cdot u = n \cdot R_L I_D = n \cdot R_L K(V_{GS} - V_t)^2,
\]
(3a)

\[
I_o = V_o / R_L = n \cdot I_D = n \cdot K(V_{GS} - V_t)^2,
\]
(3b)

where \(K\) is the process parameter of MOSFET, and \(V_t\) is the threshold voltage. Here, it is notable that both output voltage \(V_o\) and output current \(I_o\) are not...
function of source $V_S$. In other words, when the source $V_S$ is decreasing a little, such a source variation cannot affect output $V_o$ and $I_o$ immediately. Since $V_S$ is not directly connected to the load $R_L$ at any half-cycle of period, the variation of source $V_S$ will not make any immediate response on output $V_o$ and $I_o$. That is a very excellent advantage for QSC converter, so it could have better output robustness against source variation or noise. Based on the conclusion of (3), the steady-state input/output power of QSC converter can be computed as:

$$P_1 = V_S \cdot I_S = V_S \cdot I_D, \quad P_o = V_o \cdot I_o = R_L \cdot I_o^2 = V_o \cdot n \cdot I_D. \quad (4a,b)$$

Thus, using (4a)–(4b), the power conversion efficiency of converter is derived as Equation (5), where $M = V_o/V_S$ represents the voltage conversion ratio.

$$\eta = \frac{P_o}{P_1} = \frac{V_o \cdot n \cdot I_D}{V_S \cdot I_D} = n \cdot \frac{V_o}{V_S} = n \cdot M.$$ \quad (5)

Next, around some static operating point, followed by using the small-signal analysis, and consequently the small-signal transfer function of the QSC step-down converter can be suggested as:

$$G(s) = \frac{\hat{v}_o(s)}{\hat{v}_{gs}(s)} = \frac{g_m r_C r_L}{s^2 + \frac{C_o (r_C + r_L) + 2nC r_T + \eta + R_L}{2nC C_o \cdot \Delta} s + \frac{1}{2nC C_o \cdot \Delta}}, \quad (6)$$

where $\hat{i}_q = g_m \cdot \hat{v}_{gs}$, and $g_m = 2K \cdot \sqrt{I_D/K}$ is the trans-conductance. If the QSC step-down converter is regarded as an open-loop plant of control system, then its small-signal open-loop model has been derived here with two forms of: state-space and transfer function expression as (6). Next, some compensation techniques can be applied, for examples, PID compensator or state-feedback controller, to form a closed-loop feedback control system for more excellent response performances.

### 3. Control Design of CPLD-Based Converter

First of all, before the closed-loop design, let’s take a look at the stability of the open-loop QSC converter. Obviously, for the better power efficiency, the applied value of load resistance $R_L$ is supposed to be much larger than value of parasitic $r_T, r_C, r_Co$. So, the assumption of $R_L >> r_C, \quad R_L >> r_Co, \quad R_L >> r_T$ is
supposed to be accepted basically. In fact, the resistance value of load $R_L$ is about in $\Omega$-level, and the value range of parasitic $r_{T}, r_{C}, r_{Co}$ is about in $m\Omega$-level. Around some operating point of $V_{GS}$, the open-loop two-order transfer function of (6) can be approximately reduced into the open-loop one-order transfer function model with one dominant pole as:

$$G(s) = \frac{\hat{v}_o}{\hat{v}_{gs}} = \frac{n \cdot g_m \cdot R_L}{(C_o + 2nC)R_L \cdot s + 1}, \quad \text{pole}_d = -\frac{1}{(C_o + 2nC)R_L}. \quad (7a,b)$$

It is obvious that the open-loop QSC step-down converter is locally stable because this dominant pole is located in the left half of s-plane. Furthermore, the variation of operating point of $V_{GS}$ will not directly affect the location of the dominant pole, so the result almost ensures the global stability of the open-loop QSC converter. Thus, it is one of advantages that the converter scheme has an inherent good stability.

Next, let’s discuss the closed-loop control design and implementation of the QSC converter. First for steady-state regulation, according to (3a), the steady-state output voltage $V_o$ is linearly regulated by drain current $I_D$, which is controlled by the gate-source voltage $V_{GS}$. Thus, for the aim to steady-state voltage regulation, it is desired that the steady-state output voltage $V_o$ can follow reference $V_{ref}$ by adjusting the gate-source $V_{GS}$. Based on (3a), let $V_o$ be identical to the desired $V_{ref}$, and then obtain the nonlinear compensator $f$ as (8) to produce the static gate-source voltage $V_{GS}$ for achieving the steady-state regulation,

$$V_{GS} = f(V_{ref}) = \frac{V_{ref}}{nR_LK} + V_I. \quad (8)$$

Secondly for the small-signal transient regulation, according to (6), the small-signal output voltage $\hat{v}_o$ is with two-order transfer function of small-signal gate-source voltage $\hat{v}_{gs}$. Thus, for the aim to small-signal voltage regulation, it would be better to employ the closed-loop control for dynamic compensation of output $\hat{v}_o$. As the control scheme of Fig.1, a simple PI-type controller with cut-off frequency $w_L$ and proportional gain $K_P$ is applied here to compensate the transient difference between output and desired reference, even for some good performances, for example, rise time and setting time. In this PI controller, there are two parameters of $w_L, K_P$, where the gain $K_P$ is designed for tracking error.
compensation, and the cut-off frequency $w_L$ is designed for the possible high-frequency noise rejection. Therefore, combining the ideas of steady-state and transient control, the overall closed-loop control of QSC step-down DC-DC converter can be presented as shown in Fig.3, in which a voltage limiter of $v_{GS}$ is used in order to protect the drain current not to be larger than safe drain current of MOSFET.

![Fig.3 Overall closed-loop control of QSC converter](image)

Next, let’s look at CPLD controller implementation. Here, an integrated digital controller is implemented via combination with Verilog-code CPLD and ADC/DAC/OSC/OP chips to achieve the closed-loop control of QSC step-down converter with multiple output choice. From the angle of signal flow of the digital controller, the output signal $v_o$ of the converter gets in through the OP-amp low-pass filter for the high frequency noise rejection, and then the filtered analog output signal is transferred into the digital form by the ADC chip. Then, the digitalized output signal is sent into the CPLD chip and compared with desired reference $V_{ref}$, and following to produce the suitable digital-form control signal $v_{GS}$. Next, with the DAC chips, the digital-form control signal $v_{GS}$ can be transferred into the analog form for the adjustment of $i_D$. The scheme of the digital controller is shown in the Fig.1 below. In addition, the CPLD chip has to handle the timing control of the converter in accordance with the scheduled operation of Fig.2. Here, by using Verilog programming, both control signal production and timing control operation can be easily realized and integrated in this CPLD chip.

4. Experiment of CPLD-Based QSC Converter

In this section, the hardware implementation and experiment of the closed-loop CPLD-based QSC step-down DC-DC converter is illustrated. The
Implementation of CPLD-Based Quasi-Switched-Capacitor Step-Down DC-DC Converter

The hardware implementation of closed-loop QSC converter is shown in the photo of Fig.4, and all the hardware elements are listed in Table 1. Here, the core: CPLD chip has to not only handle the control signal production, but also realize the timing control operation as Fig.2. So, by using Verilog programming, both the goals can be easily achieved and integrated in this CPLD chip, and Appendix deals with the embedded Verilog code of CPLD digital controller, where there are 8 output/input terminals planned as shown in Fig.5, and their functions/behaviors are described in Table 2. To deserve to be mentioned, it’s not easy to realize square-root computation of nonlinear compensation as Equation (8) in the CPLD chip. So, the table-look-up method is employed here to produce the static control signal $V_{GS}$ for the different reference $V_{ref}$, i.e., the static $V_{GS}$ can be computed for the different $V_{ref}$, and stored in the program in advance, as the declared parameters: v5,v3, and v2 in Appendix. Here, the cut-off frequency $w_L$ is taken by 1470rad/sec, i.e. 234Hz, for the high-frequency noise reduction. In addition, the different gain $K_P$ can be designed for the different output choice, where $K_P$ is set on the values of 8/8/6 for the desired output voltage of 5V/3.3V/2V respectively, as shown in Appendix. The hardware implementation of the closed-loop CPLD-based QSC step-down converter of Fig.4 is with the circuit-layout size of $12cm \times 8cm$, and the wires of the circuit board is made by the prototype circuit-carving machine. For checking closed-loop performance, some experiments are discussed and measured (Tool: Tektronix Oscilloscope TDS 210), including: (A). voltage conversion and output ripple percentage, and (B). output robustness against source variation.
Fig. 4 Hardware implementation of CPLD-based QSC step-down converter with multiple output choice

Table 1. Hardware elements of CPLD-based converter

<table>
<thead>
<tr>
<th>Component</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRF510(NMOS) x 2</td>
<td></td>
</tr>
<tr>
<td>J77(PMOS) x 2</td>
<td></td>
</tr>
<tr>
<td>33uf x 3</td>
<td></td>
</tr>
<tr>
<td>47uf x 1</td>
<td></td>
</tr>
<tr>
<td>1.8402MHz Crystal x 1</td>
<td></td>
</tr>
<tr>
<td>CPLD XC9572 x 1</td>
<td></td>
</tr>
<tr>
<td>ADC0804(ADC) x 1</td>
<td></td>
</tr>
<tr>
<td>DAC0800(DAC) x 2</td>
<td></td>
</tr>
<tr>
<td>HA17741(OP amp) x 6</td>
<td></td>
</tr>
<tr>
<td>DIP 2bit x 1</td>
<td></td>
</tr>
</tbody>
</table>

Table 2. Terminals of Verilog-code-based CPLD

<table>
<thead>
<tr>
<th>Terminal name</th>
<th>Bit</th>
<th>I/O</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK</td>
<td>1</td>
<td>Input</td>
<td>Input for clock signal from the crystal oscillator</td>
</tr>
<tr>
<td>SEL1</td>
<td>1</td>
<td>Input</td>
<td>Selection input 1 for multiple output choice</td>
</tr>
<tr>
<td>SEL2</td>
<td>1</td>
<td>Input</td>
<td>Selection input 2 for multiple output choice</td>
</tr>
<tr>
<td>VO[7:0]</td>
<td>8</td>
<td>Input</td>
<td>Input for the filtered digitalized output from ADC</td>
</tr>
<tr>
<td>OUTN1</td>
<td>1</td>
<td>Output</td>
<td>Output for the control of MOSFET SA</td>
</tr>
<tr>
<td>OUTN2</td>
<td>1</td>
<td>Output</td>
<td>Output for the control of MOSFET SB</td>
</tr>
<tr>
<td>OUTADC1[7:0]</td>
<td>8</td>
<td>Output</td>
<td>Output for the control of MOSFET QSA to DAC</td>
</tr>
<tr>
<td>OUTADC2[7:0]</td>
<td>8</td>
<td>Output</td>
<td>Output for the control of MOSFET QSB to DAC</td>
</tr>
</tbody>
</table>
Fig.5 Terminals of CPLD controller

(A). First, the QSC step-down converter is operated from source $V_S$ of 9V conversion into output $V_o$ of 2V ($V_{ref}=2V$) for supplying the load $R_L$ of 200Ω at the switching frequency of 12.5kHz. The steady-state output conversion is measured as shown in Fig.6(a). It is obvious that the conversion works stably, and the output ripple percentage can be measured and computed as:

$$rp = \frac{\Delta V_o}{V_o} = 1.51\%.$$

Here, for simplifying hardware implementation, the stage number $n$ is only taken by one ($n=1$), but it results in the bad efficiency about 22% indeed. In order to improve the power efficiency, it is practicable to increase or change the stage number $n$ for the better efficiency. According to the theoretical conclusion of (5), the efficiency is enhanced up to 66% while the stage number $n$ is three ($n=3$), or further, the efficiency can be improved to 88% while number $n$ is taken by four ($n=4$). Besides, for the other output choices ($V_{ref}=3.3V, 5V$), the steady outputs are measured as shown in Fig.6(b)–(c). It is obvious that the conversions still work stably, and the relative output ripple percentages are measured as: 1.78% and 1.01%, respectively. These results show that the QSC converter hardware has a pretty good steady-state performance.

(B). Secondly, since the source voltage is decreasing naturally with increasing running time of battery, or varying from the bad-quality battery, the output robustness against the source noises must be considered and emphasized. Here, it is applied to the hardware that source $V_S$ has the average value of 8V and extra 0.5V pulse noise as shown in Fig.7(a) above. Then, the output voltage $V_o$ is measured as shown in Fig. 7(a) below, and it is found that output $V_o$ is still following the reference $V_{ref}$ to supply output of 2V, even though source $V_S$ has the smaller than standard source of 9V and the pulse disturbance. Besides, for the other output choices ($V_{ref}=3.3V, 5V$), the output robustness can be also experimented and measured as shown in Fig.7(b)–(c). In these figures, it is found that this converter can still firmly supply the outputs of 3.3V, 5V respectively in spite of the source variation. So, the closed-loop QSC converter has a good robustness against source noises.
Fig. 6(a) Steady output conversion (9V/2V)

Fig. 6(b) Steady output conversion (9V/3.3V)

Fig. 6(c) Steady output conversion (9V/5V)

Fig. 7(a) Steady output while source variation (9V/2V)

Fig. 7(b) Steady output while source variation (9V/3.3V)

Fig. 7(c) Steady output while source variation (9V/5V)
5. Conclusion

A simple QSC step-down DC-DC converter with multiple output choice (9V/5V, 9V/3.3V, 9V/2V) is implemented by using CPLD-based digital controller for a variety of low-power output requirement (Specification: Input voltage: 7.0V~9.0V, load range: 50~400Ohms). In this paper, an integrated digital controller is designed and implemented via combination with Verilog-code CPLD and ADC/DAC chips to achieve the closed-loop control of QSC step-down DC-DC converter. Such a Verilog-based CPLD can make controller design more flexible, simple and reliable. Finally, the hardware experiments are illustrated to show the efficacy of the scheme, where some cases include: voltage conversion and output ripple percentage, and output robustness against source variation. The following advantages of the proposed scheme are involved. (i) Since all the elements of QSC converter only contain MOSFETS and capacitors, the uniform is helpful to I.C. fabrication future. (ii) An interleaved current-mode control is employed from battery source interleaved charging to the series capacitors of the different cells by the controlled current source, so the continuous input current comes into being, and then it results in a good feature: low EMI. (iii) Such a Verilog-code-based CPLD chip here can really make the controller design of QSC converter more flexible, simple and reliable. (iv) Due to high-frequency operation, it results possibly in low output voltage ripple. (v) Since source $V_S$ is not directly connected to the load $R_L$ any time, the source variation will not make any immediate response on output $V_o$ and $I_o$. So, it could be with the better output robustness against source variation or noise. (vi) Since two cells are complementarily working in anti-phase, i.e., the duty cycle is fixed at 0.5, such a constant duty cycle is much useful especially to control design and theoretical analysis of the converter. (vii) The dominant pole is located in the left half of s-plane, so it is obvious that the open-loop converter is locally stable. Thus, this scheme has an inherent good stability.
APPENDIX: VERILOG CODE OF CPLD-BASED CONTROLLER

//Definition/
module Switch(clk,vo,outadc1,outadc2,outn1,outn2,sel1,sel2)
  input clk,sel1,sel2;
  input [7:0] vo;
  output [7:0] outadc1,outadc2;
  output outn1,outn2;
  reg [7:0] outadc1,outadc2,vdata,vr;
  reg outn1,outn2;
  reg flag;
  reg [3:0]tmp;
  parameter v5=8'hac,v3=8'hb4,v2=8'hc0;
//Table-look-up//
always @(negedge clk)
begin
  case ( {sel2,sel1})
    //O/P Choice: 5V//
    2'b00:
      begin
        if(vo <= 8'h0f)
          begin
            vdata = 8'h01;
          end
        else if(vo >= 8'hff)
          begin
            vdata = 8'hff;
          end
        else
          begin
            if(vo <= 8'h9f)
              begin
                vr=(8'hfa-vo)*8;
                vdata = v5-vr;
              end
            else if(vo >= 8'hfb)
              begin
                vr=(vo-8'hfb)*8;
                vdata = v5+vr;
              end
          end
    end
    //O/P Choice: 3.3V//
    2'b01:
      begin
        if(vo <= 8'h93)
          begin
            vdata = 8'h01;
          end
        else if(vo >= 8'h9b2)
          begin
            vdata = 8'hff;
          end
        else
          begin
            if(vo <= 8'hA5)
              begin
                vr=(8'hA5-vo)*8;
                vdata = v3-vr;
              end
            else if(vo >= 8'hA9)
              begin
                vr=(vo-8'hA9)*8;
                vdata = v3+vr;
              end
          end
    end
    //O/P Choice: 2V//
    2'b10:
      begin
        if(vo <= 8'h4c)
          begin
            vdata=8'h01;
          end
        else if(vo >= 8'h70)
          begin
            vdata=8'hff;
          end
        else
          begin
            vr=(8'h63-vo)*6;
            vdata=2-vr;
          end
        end
    end
    //Gain: Kp=6//
    2'b11: vdata = vo;
  endcase
//Timing Control//
  tmp=tmp+1;
  if(tmp==6 && flag==0)
    begin
      outn2=~outn2;
    end
  if(tmp==6 && flag==1)
    begin
      outn1=~outn1;
    end
  if(tmp==2 && flag==1)
    begin
      outadc2=vdata;
    end
  if(tmp==2 && flag==0)
    begin
      outadc1=vdata;
    end
  if(tmp==7)
    begin
      flag=~flag;
      if(flag==1)
        begin
          outadc1=8'hff;
          outn1=~outn1;
        end
      if(flag==0)
        begin
          outadc2=8'hff;
          outn2=~outn2;
        end
    end
    tmp=0;
  end
endmodule
References


以 CPLD 為主之擬切換式電容降壓型直流轉換器的實作

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摘 要

本文以複合性可程式邏輯元件(CPLD)為控制器實現主體，設計並實作一簡易的擬切換式電容(QSC)降壓型直流轉換器，其具有多重電壓輸出選擇(9V/5V, 3.3V, 2V)，並用於低功率應用(Input: 7.0~9.0V, Load: 50~400Ohms)。其中數位控制器主要是由 CPLD 及 ADC/DAC 等晶片所合成，以提供閉迴路控制之用。如此的硬體描述語言(Verilog)可以使得控制器的設計更為有彈性、簡單及可靠。事實上，SC 電路並不需要任何電感性元件，因此極有助於未來 VLSI 積體電路設計與製程之實現。本文 QSC 轉換器架構採用交錯式電流模式控制，其作法是由電池電源端以交錯的方式，對子電路中的電容進行串聯充電(以壓控電流源方式充電)，因此在電源端能出現連續的電源端電流，這會使得電路有較小的電磁干擾現象。此外如此的電流控制模式，不僅會能增強輸出電壓受電源端雜訊干擾的強健能力，且可保有對負載變化時的調整能力。最後本文以實作的 QSC 硬體，來進行實際的量測，其各项實作結果可以驗證所提結論之正確性與有效性，其中包含有輸出入電壓比、輸出電壓漣波百分比、及輸出端對電源端干擾之強健性。

關鍵詞：擬切換式電容，降壓型，直流轉換器，硬體描述語言，複合性可程式邏輯元件。